CHAPTER VIII

OPERATIONAL-AMPLIFIER DESIGN TECHNIQUES

8.1 INTRODUCTION

This chapter introduces some of the circuit configurations that are used for the design of high-performance operational amplifiers. This brief exposure cannot make operational-amplifier designers of us all, since considerable experience coupled with a sprinkling of witchcraft seems essential to the design process. Fortunately, there is little need to become highly proficient in this area, since a continuously updated assortment of excellent designs is available commercially. However, the optimum performance can only be obtained from these circuits when their capabilities and limitations are appreciated. Furthermore, this is an area where good design practice has evolved to a remarkable degree, and the techniques used for operational-amplifier design are often valuable in other applications.

The input stage of an operational amplifier usually consists of a bipolar-transistor differential amplifier that provides the differential input connection and the low drift essential in many applications. The design of this type of amplifier was investigated in detail in Chapter 7. The input stage is normally followed by one or more intermediate stages that combine with it to provide the voltage gain of the amplifier. Some type of buffer amplifier that isolates the final voltage-gain stage from loads and provides low output impedance completes the design. Configurations that are used for the intermediate and output stages are described in this chapter.

The interplay between a number of conflicting design considerations leads to a complete circuit that reflects a number of engineering compromises. For example, one simple way to provide the high voltage gain characteristic of operational amplifiers is to use several voltage-gain stages. However, we shall see that the use of multiple gain stages complicates the problem of insuring stability in a variety of feedback connections. Similarly, the dynamics of an amplifier are normally improved by operation at higher quiescent current levels, since the frequency response of transistors increases with increasing bias current until quite high levels are reached. However,

operation at higher current levels deteriorates d-c performance characteristics. Some of the guidelines used to resolve these and other design conflicts are outlined in this chapter and illustrated by the example circuit described in Chapter 9.

8.2 AMPLIFIER TOPOLOGIES

Requirements usually constrain the input and output stages of an operational amplifier to be a differential amplifier and some type of buffer (normally an emitter-follower connection), respectively.

It is in the intermediate stage or stages that design flexibility is evident, and the difference in performance between a good and a poor circuit often reflects the differences in intermediate-stage design. The primary performance objective is that this portion of the circuit provide high voltage gain coupled with a transfer function that permits stable, wide-band behavior in a variety of feedback connections. Furthermore, the flexibility of easily and predictably modifying the amplifier open-loop transfer function in order to optimize it for a particular feedback connection is desirable for a general-purpose design.

8.2.1 A Design with Three Voltage-Gain Stages

One much-too-frequently used design is shown in simplified form in Fig. 8.1. The path labeled feedforward is one technique used to stabilize the amplifier, and is not essential to the initial description of operation. The basic circuit uses a differential input since this connection is mandatory for low drift and high common-mode rejection ratio. Two common-emitter stages (transistors Q_3 and Q_4) are used to provide the high voltage gain characteristic of operational amplifiers. Some sort of buffer amplifier (shown diagrammatically as the unity-gain amplifier in the output portion) is used to provide the required output characteristics.

Casual inspection indicates some merit for the design of Fig. 8.1. Low drift is possible and d-c gains in excess of 10^5 can be achieved. The difficulty is evident only when the dynamics of the amplifier are examined. The transfer function $V_o(s)/[V_{i2}(s) - V_{i1}(s)]$ determines stability in feedback connections. With typical element values, this transfer function has three or four poles located within a two-to-three decade range of frequency. It is not possible to achieve large loop-transmission magnitude and simultaneously to maintain stability with this type of transfer function. The designer of this type of amplifier should be discouraged when he compares his circuit with that of a phase-shift oscillator, where negative feedback is applied around three or more closely spaced poles.

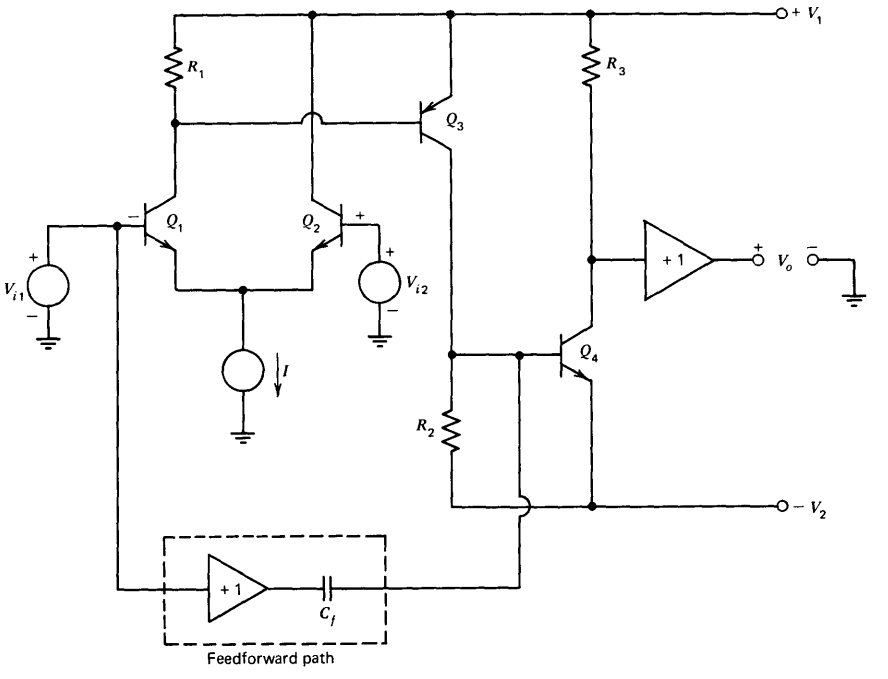

Figure 8.1 One approach to operational-amplifier design.

The problem can be illustrated by computing the transfer function for the amplifier shown in Fig. 8.1 with component values listed in Table 8.1. The reasons for selecting these component values are as follows. Fifteen-volt supplies are used since this value has become the standard for many solid-state operational amplifiers. The quiescent operating current of the first stage is low to reduce input bias current.

Relatively modest increases in quiescent currents from stage-to-stage are used to minimize loading effects. At these levels, circuit impedances are such that little change in the transfer function results if r_x is assumed equal to zero. However, r_x has been retained for completeness. Junction capacitances are dominated by space-charge layer effects at low operating currents, so equal values for all transistor capacitances have been assumed. Clearly any equal change in all capacitances simply frequency scales the transfer function. The resistors in the base circuits of Q_3 and Q_4 are assumed large to maximize d-c gain. In practice, current sources can be used to maintain high incremental resistance and to establish bias currents. Resistor R_3 is chosen to yield a quiescent output voltage equal to zero.

Table 8.1. Parameter Values for Example Using Amplifier of Fig. 8.1

Supply voltages:

± 15 V

Bias currents:

$I_{C1} = I_{C2} = 10\ \mu A$
$I_{C3} = 50\ \mu A$
$I_{C4} = 250\ \mu A$

Transconductances[a] implied by bias currents:

$g_{m1} = g_{m2} = 4 \times 10^{-4}$ mho
$g_{m3} = 2 \times 10^{-3}$ mho
$g_{m4} = 10^{-2}$ mho

Other transistor parameters:

$\beta = 100$ (all transistors)
$r_{\pi 1} = r_{\pi 2} = 250\ k\Omega$
$r_{\pi 3} = 50\ k\Omega$
$r_{\pi 4} = 10\ k\Omega$
$r_x = 100\ \Omega$ (all transistors)
$C_\mu = C_\pi = 10$ pF (all transistors)

Reisistors:

R_1 and R_2 large compared to $r_{\pi 3}$ and $r_{\pi 4}$, respectively.
$R_3 = 60\ k\Omega$

(Satisfying the inequalities normally requires that current sources be used rather than resistors in practical designs.)

Buffer amplifier assumed to have infinite input impedance.

[a] Recall that for any bipolar transistor operating at current levels where ohmic drops are unimportant, the transconductance is related to quiescent collector current by $g_m = q|I_C|/kT \simeq 40\ V^{-1}|I_C|$ at room temperature.

A computer-generated transfer function $V_o(j\omega)/[V_{i2}(j\omega) - V_{i1}(j\omega)]$ for this amplifier is shown in Bode-plot form in Fig. 8.2.[1] Two important features of this transfer function are easily related to circuit parameters. The low-frequency gain can be determined by inspection. Invoking the usual assump-

[1] The gains of the amplifier for signals applied to its two inputs are not identical at high frequencies because a fraction of the signal applied to the base of Q_1 is coupled directly to the base of Q_3 via the collector-to-base capacitance of Q_1. This effect, which is insignificant until frequencies approaching the f_T's of the transistors used in the circuit, has been ignored in calculating the amplifier transfer function so that a true differential gain expression results.

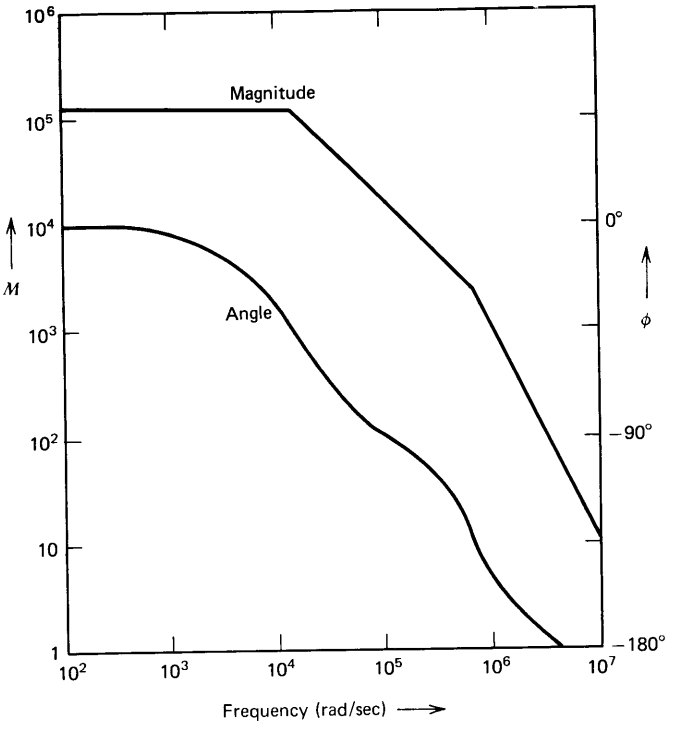

Figure 8.2 Transfer function for amplifier of Fig. 8.1.

tions, the incremental changes in first-stage collector current is related to an incremental change in differential input voltage as

$$i_{c1} = -\left(\frac{v_{i2} - v_{i1}}{1/g_{m1} + 1/g_{m2}}\right) \tag{8.1}$$

Since R_1 is large compared to the input resistance of Q_3, all of this incremental current flows into the base of Q_3. This base current is amplified by a factor of β_3, and resulting incremental current flows into the base of Q_4. The incremental output voltage becomes

$$v_o = -i_{c1}\beta_3\beta_4 R_3 \tag{8.2}$$

combining Eqns. 8.1 and 8.2 shows that the low-frequency voltage gain is

$$\frac{v_o}{v_{i2} - v_{i1}} = \frac{\beta_3\beta_4 R_3}{(1/g_{m1} + 1/g_{m2})} \tag{8.3}$$

Substituting parameter values from Table 8.1 into this equation shows that the incremental d-c gain is 1.2×10^5.

The lowest frequency pole plotted in Fig. 8.1 has a break frequency of 1.36×10^4 radians per second. This pole results from feedback through the collector-to-base capacitance of Q_4 (sometimes called Miller effect), as shown by the following development. An incremental model that can be used to evaluate the transimpedance of the final common-emitter stage is shown in Fig. 8.3. This transimpedance is a multiplicative term in the complete amplifier transfer function.

Node equations for this circuit are

$$\begin{aligned} -I_{c3} &= [g_{\pi 4} + (C_{\mu 4} + C_{\pi 4})s]V_a - C_{\mu 4}sV_o \\ 0 &= (g_{m4} - C_{\mu 4})sV_a + (G_3 + C_{\mu 4}s)V_o \end{aligned} \tag{8.4}$$

Solving for the transimpedance shows that

$$\frac{V_o(s)}{I_{c3}(s)} = \frac{\beta R_3[-(C_{\mu 4}/g_{m4})s + 1]}{r_{\pi 4}R_3C_{\mu 4}C_{\pi 4}s^2 + r_{\pi 4}\{[(g_{m4} + g_{\pi 4})R_3 + 1]C_{\mu 4} + C_{\pi 4}\}s + 1} \tag{8.5}$$

The denominator of Eqn. 8.5 is normally dominated by the term that includes the factor $g_{m4}R_3C_{\mu 4}$, reflecting the importance of feedback through $C_{\mu 4}$. Substituting values from Table 8.1 into Eqn. 8.5 and factoring the denominator polynominal results in

$$\frac{V_o(s)}{I_{c3}(s)} = \frac{6 \times 10^6(-10^{-9}s + 1)}{(10^{-9}s + 1)(6.08 \times 10^{-5}s + 1)} \tag{8.6}$$

This development shows that the output stage would have a dominant pole with a 1.64×10^4 radians-per-second break frequency in its transfer function if the other components in the circuit did not alter the location of this pole. This value agrees with the location of the dominant pole for the complete amplifier within approximately 20%.

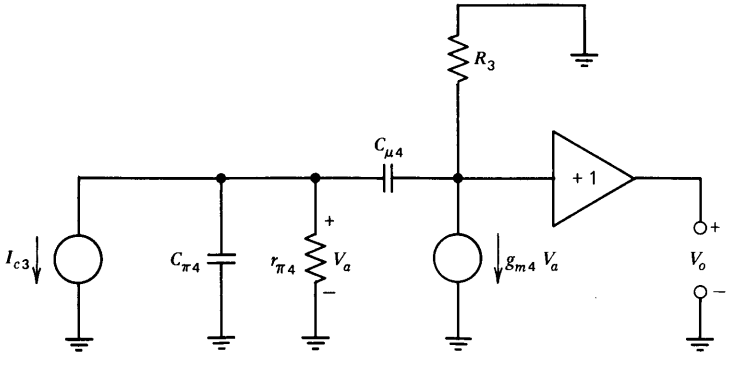

Figure 8.3 Model used to determine dynamics of final common-emitter stage of three-stage amplifier.

The algebra involved in getting this result can be circumvented by recognizing that a one-pole[2] (or Miller-effect) approximation to the input capacitance of transistor Q_4 predicts a value

$$C_T = C_{\pi 4} + C_{\mu 4}(1 + g_{m4}R_3) \tag{8.7}$$

The break frequency estimated at this node is

$$\omega_h = \frac{1}{r_{\pi 4}C_T} = 1.66 \times 10^4 \text{ rad/sec} \tag{8.8}$$

While the d-c gain and the dominant pole location for this configuration are easily estimated, the location of other transfer-function singularities are related to amplifier parameters in a more complex way.

The essential feature to be gained from the Bode plot of Fig. 8.2 is that this transfer function is far from ideal for use in many feedback connections. The amplifier is hopelessly unstable if it is operated with its noninverting input connected to an incremental ground and a wire connecting its output to its inverting input, creating a loop with a as shown in the Bode plot and $f = 1$. In fact, if frequency-independent feedback is applied around the amplifier, it is necessary to reduce the magnitude of the loop transmission by a factor of 50 below the gain of the amplifier itself to make it stable in an absolute sense, and by a factor of 2000 to obtain 45° of phase margin. The required attenuation could be obtained by means of resistively shunting the input of the amplifier or through the use of a lag network (see Section 5.2.4). Either of these approaches severely compromises desensitivity and noise performance in many applications because of the large attenuation necessary for stability. Better results can normally be obtained by modifying the dynamics of the amplifier itself.

8.2.2 Compensating Three-Stage Amplifiers

At least two methods are often used to improve the dynamics of an amplifier similar to that described in the previous section. One of these approaches recognizes that the poles in the amplifier can be modeled as occurring because of R-C circuits located at various amplifier nodes. This type of association was made in the previous section for the dominant amplifier pole. The transfer function for a gain stage includes a multiplicative term of the general form $R_e/(R_eC_eS + 1)$, where R_e and C_e are the effective resistance and capacitance at a particular node (see Fig. 8.4). If a com-

[2] P. E. Gray and C. L. Searle, *Electronic Principles: Physics, Models, and Circuits*, Wiley, New York, 1969, pp. 497–503.

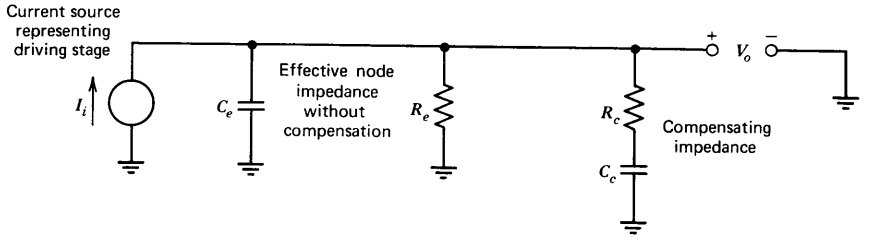

Figure 8.4 Compensation by adding a shunt impedance.

pensating series R-C network to ground consisting of a resistor $R_c \ll R_e$ and a capacitor $C_c \gg C_e$ is added, the transfer function becomes

$$\frac{V_o(s)}{I_i(s)} \simeq \frac{R_e(R_cC_cs + 1)}{(R_eC_cs + 1)(R_cC_es + 1)} \tag{8.9}$$

The single pole has been replaced by two poles and a zero. (Note that asymptotic behavior at high and low frequencies, which is controlled by R_e and C_c, has not been changed.) Component values are chosen so that one pole occurs at a much lower frequency than the original pole and the other at a frequency above the unity-gain frequency of the complete amplifier, as illustrated in Fig. 8.5. The positive phase shift of the zero often can improve the phase margin of the amplifier. This type of compensation can be viewed as one of combining the uncompensated transfer function with appropriately located lag and lead transfer functions. While the singularities must be related so that the compensated and uncompensated transfer functions are identical at very low and very high frequencies, the second pole can always be moved to arbitrarily high frequencies by locating the first pole at a sufficiently low frequency.

An alternative way to view this type of compensation is shown in the s-plane diagrams of Fig. 8.6. It is assumed that the three-stage amplifier has three poles at frequencies of interest. The lowest-frequency pole of the triad is replaced by two poles and a zero by means of a shunt R-C network. One possible way to choose singularity locations is to use the zero to cancel the second pole in the original transfer function and to locate the high-frequency pole that results from compensation above the highest-frequency original pole. The net effect of this type of compensation is to increase the separation of the poles so that greater desensitivity can be achieved for a given relative stability.

Several variations of the basic compensation scheme exist. It is possible to realize similar kinds of transfer functions by connecting a series R-C network from collector to base of a transistor rather than from its base to

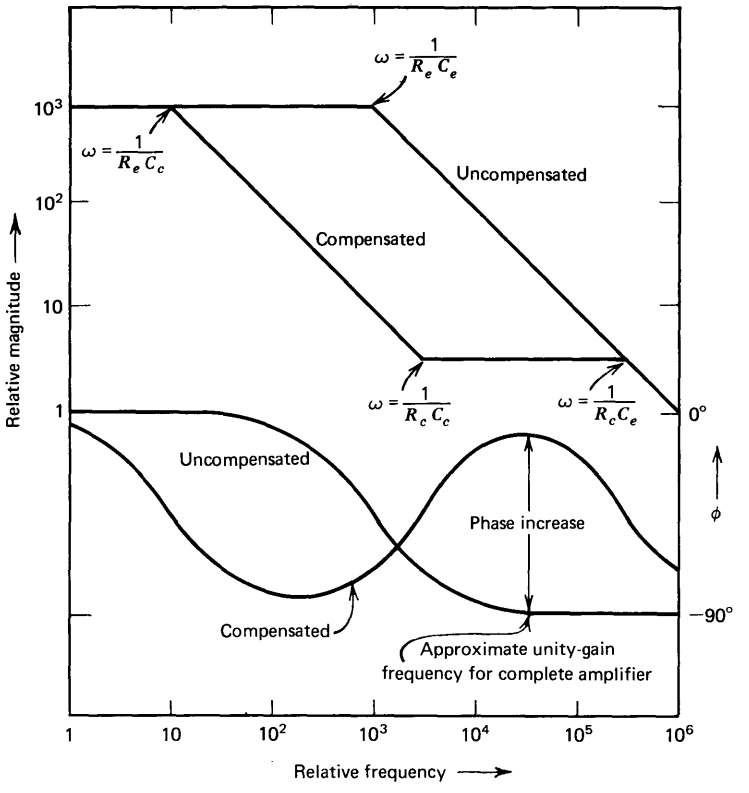

Figure 8.5 Effect of adding a shunt impedance on the transfer function of one stage.

an incrementally-grounded point. The same kind of compensation can be used at more than one node, and this multiple compensation is frequently required in more complex amplifiers.

While this general type of compensation is effective and has been successfully applied to a number of amplifier designs, it is less than ideal for several reasons. One of the more important considerations is that the determination of element values that result in a given transfer function requires rather involved calculations. This difficulty tends to discourage the user from finding the optimum compensating-element values for use in other than standard applications. This type of compensation also requires large capacitors (typically 1000 pF to 0.1 μF) when the network is shunted from base to an incremental ground. The energy storage of a large capacitor can delay recovery following an amplifier overload that charges the capacitor to the wrong voltage level.

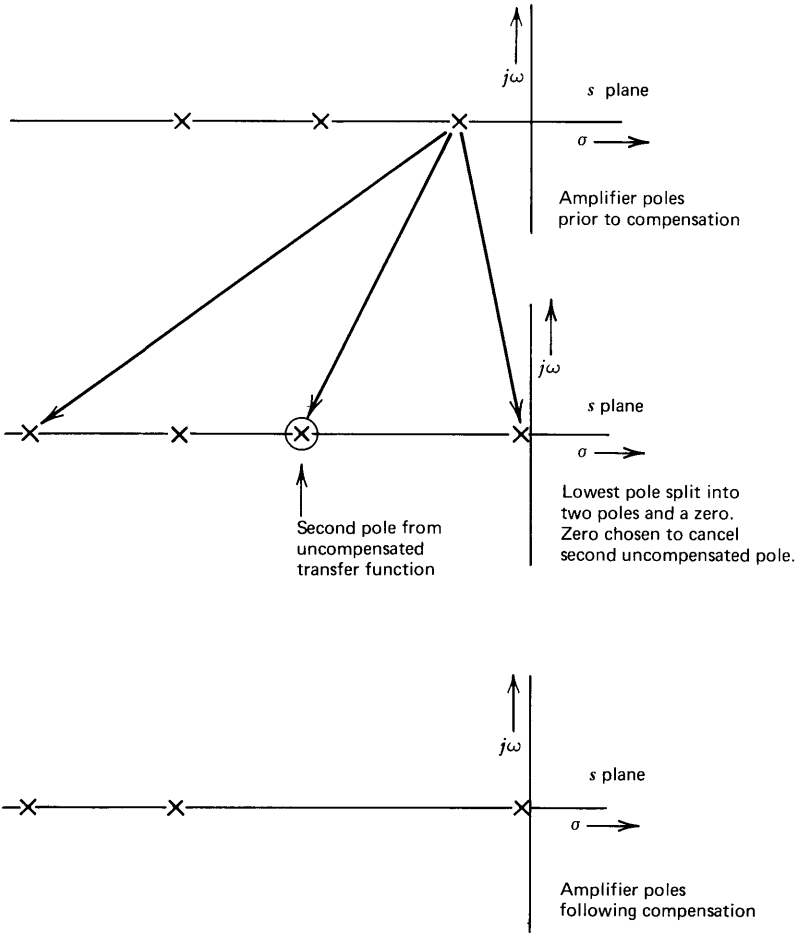

Figure 8.6 *s*-plane plots illustrating effect of shunt impedance on three-stage amplifier transfer function.

An alternative type of compensation that may be used alone or in conjunction with a shunt impedance is to "feed forward" around one or more amplifier stages as shown in Fig. 8.1. Here a unity-voltage-gain buffer amplifier (not essential but included in some designs to prevent loading at the inverting input terminal) couples the input signal to the base of Q_4 through capacitor C_f. Since the first stages are bypassed at high frequency, the high-frequency dynamics of the operational amplifier should be essentially those of the output stage. The hope is that the output stage has only

one pole at frequencies of interest, and therefore will be stable with any amount of frequency-independent feedback.

Feedforward is not without its disadvantages. The frequency response of a feedforward amplifier is significantly lower for signals applied to the noninverting input than for signals applied to its inverting input. Thus the amplifier has severely reduced bandwidth when used in noninverting connections. There are also problems that stem from the type of transfer functions that result from feedforward compensation. There is usually a second- or third-order rolloff at low frequencies, with the transfer function recovering to first order in the vicinity of the unity-gain frequency. Since this transfer function resembles those obtained with lag compensation, the settling time may be relatively long because of the small amplitude "tails" that can result with lag compensation (see Section 5.2.6). It is also possible to have these amplifiers become conditionally stable in certain connections (Section 6.3.4). This topic is investigated in Problem P8.3.

Before leaving the subject of three-stage amplifiers, the liberty that has been taken in the definition of a stage is worth noting. The stages are never as simple as those shown in Fig. 8.1. The essential feature that characterizes a voltage-gain stage is that it generally introduces one pole at moderate frequencies. The 709 (Fig. 8.7) is an example of an early integrated-circuit amplifier that is a three-stage design. While we do not intend to investigate the operation of this circuit in detail (several modern and more useful amplifiers are described in Chapter 10), the basic signal-flow path illustrates the three-stage nature of this design. Transistors Q_1 and Q_2 form a differential amplifier. The main second-stage amplification occurs through the Q_4-Q_6 Darlington-connected pair. Transistors Q_3 and Q_5 complete a differential second stage with the Q_4-Q_6 pair and are included primarily to reduce amplifier drift. Transistors Q_8 and Q_9 are used for level shifting, with common-emitter stage Q_{12} the final stage of voltage gain. Emitter followers Q_{13} and Q_{14} function as a buffer amplifier. There is some minor-loop feedback applied around the output stage to linearize its performance and to modify its dynamics via R_{15}.

Compensation is implemented by connecting a series R-C network from the output to the input of the second stage. It is also necessary to use capacitive feedback from the amplifier output to the base of Q_{12} (essentially around the output stage) to obtain acceptable stability in most applications.

8.2.3 A Two-Stage Design

While a number of operational-amplifier designs with three (or even more) voltage amplifying stages exist, it is hard to escape the conclusion that one is fighting nature when he tries to stabilize an amplifier with three

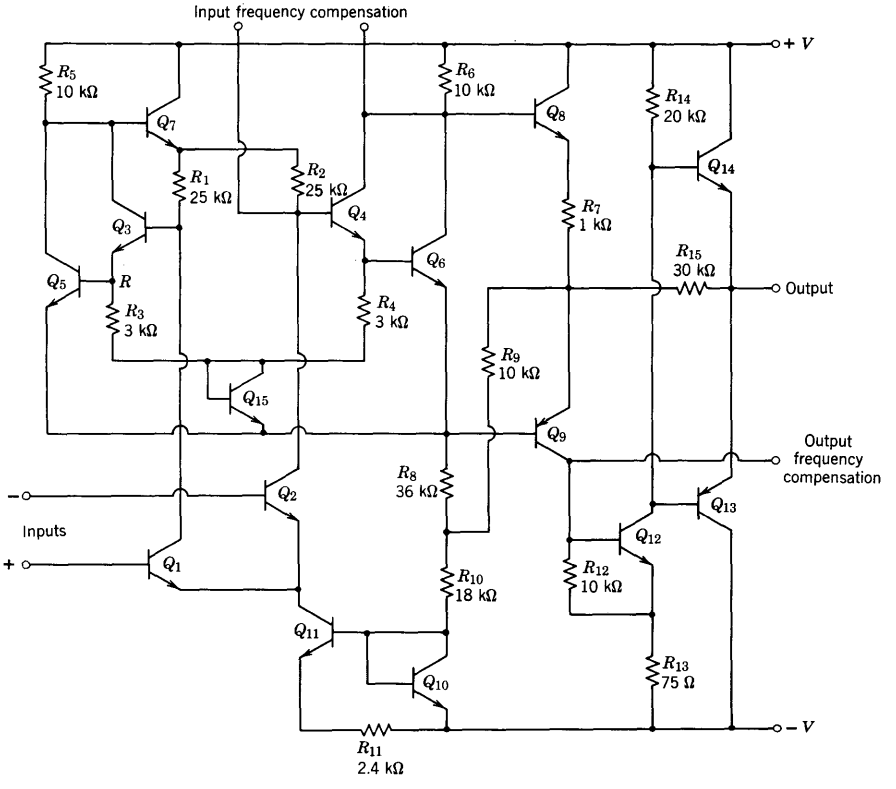

Figure 8.7 The 709 integrated-circuit operational amplifier.

or more closely spaced poles. The key to successful operational-amplifier design is to realize that the only really effective way to eliminate poles in an amplifier transfer function is to reduce the number of voltage-gain producing stages. Stages that provide current gain only, such as emitter followers, generally have poles located at high enough frequencies to be ignored.

An amplifier with two voltage-gain stages results if one of the common-emitter stages of Fig. 8.1 is eliminated, as shown in Fig. 8.8.[3] Again, transistors Q_1 and Q_2 function as a differential amplifier. However, in contrast to the previous amplifier, note that the base of transistor Q_1 is the inverting input of the complete amplifier, while the first-stage output is the collector

[3] The great value and versatility of this basic amplifier and its many variations were first pointed out to me by Dr. F. W. Sarles, Jr.

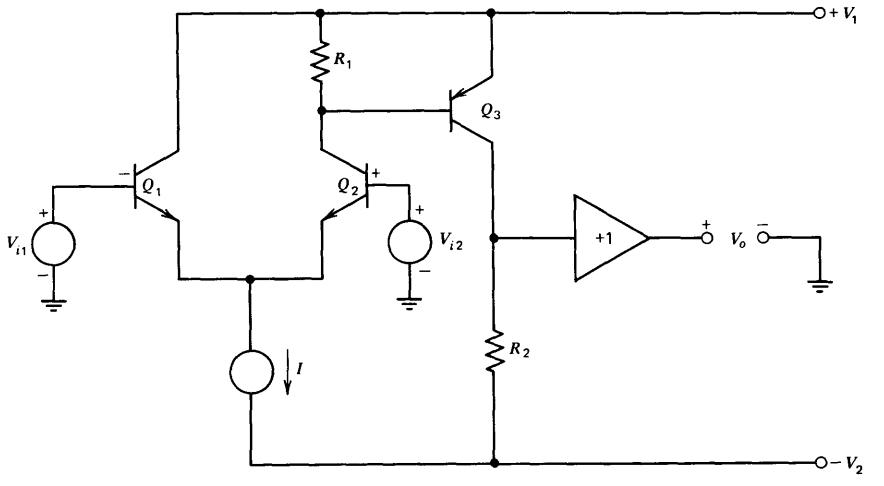

Figure 8.8 Basic two-stage amplifier.

of transistor Q_2. This emitter-coupled connection assures low input capacitance (approximately $C_{\mu 1} + C_{\pi 1}/2$) at the base of Q_1 since this device is operating as an emitter follower. Low input capacitance is an advantage in many applications since feedback is normally applied from the output of the amplifier to its inverting input terminal. The input capacitance at the inverting input can introduce an additional moderate-frequency pole in the loop transmission of the amplifier-feedback network combination with attendant stability problems. Thus low input capacitance increases the range of feedback impedances that can be used without deteriorating the loop transmission.

The transfer function for this amplifier calculated using the parameter values in Table 8.2 is[4]

$$\frac{V_o(s)}{V_{i2}(s) - V_{i1}(s)} = \frac{6 \times 10^3}{(3 \times 10^{-4}s + 1)(1.1 \times 10^{-8}s + 1)} \tag{8.10}$$

with all other singularities above 5×10^8 sec^{-1}. The corresponding Bode plot (Fig. 8.9) shows that a phase margin of 75° results even when the out-

[4] As in the case of the three-stage amplifier, the slight input-stage unbalance that occurs at high frequencies because of signals fed directly to the base of Q_3 via the collector-to-base capacitance of Q_2 has been ignored in the analysis that leads to this transfer function. The error introduced by this simplification is insignificant at frequencies below the unity-gain frequency of the amplifier. Furthermore, the transfer function of interest in most feedback applications where the feedback signal is applied to the base of Q_1 does not include the feed-forward term associated with $C_{\mu 2}$.

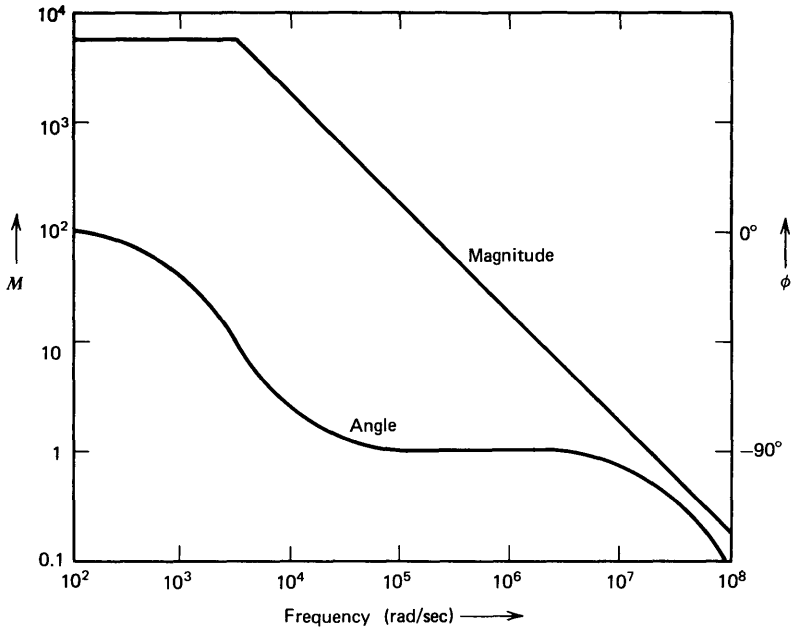

Figure 8.9 Transfer function of two-stage amplifier.

put of the amplifier is fed directly back to its inverting input. This type of transfer function, obtained without including any additional compensation components, contrasts sharply with the uncompensated three-stage-amplifier transfer function of the previous section.

It is informative to see why the transfer function of this amplifier is dominated by a single pole and why the second pole is separated from the dominant pole by a factor of approximately 30,000. This separation, which permits excellent desensitivity in feedback applications while maintaining good relative stability, is a major advantage attributable to the two-stage design. The dominant pole is primarily a result of energy storage in the collector-to-base capacitance of transistor Q_3. A C_T approximation to the input capacitance of this transistor is (see the discussion associated with Eqn. 8.7)

$$C_T = C_{\pi 3} + C_{\mu 3}(1 + g_{m3}R_2) = 6.02 \times 10^{-9}\,\text{F} \tag{8.11}$$

The corresponding time constant

$$\tau_{B3} = C_T r_{\pi 3} = 3.01 \times 10^{-4}\,\text{sec} \tag{8.12}$$

agrees with the dominant time constant in Eqn. 8.10. The essential point is that the feedback through $C_{\mu 3}$, which is actually a form of minor loop compensation (see Section 5.3), controls the transfer function of the com-

Table 8.2 Parameter Values for Example Using Amplifier of Fig. 8.8

Supply voltages:

± 15 V

Bias currents:

$I_{C1} = I_{C2} = 10\ \mu A$
$I_{C3} = 50\ \mu A$

Transconductances implied by bias currents:

$g_{m1} = g_{m2} = 4 \times 10^{-4}$ mho
$g_{m3} = 2 \times 10^{-3}$ mho

Other transistor parameters:

$\beta = 100$ (all transistors)
$r_{\pi 1} = r_{\pi 2} = 250\ k\Omega$
$r_{\pi 3} = 50\ k\Omega$
$r_x = 100\ \Omega$ (all transistors)
$C_\mu = C_\pi = 10$ pF (all transistors)

Resistors:

$R_1 \gg r_{\pi 3}$
$R_2 = 300\ k\Omega$

Buffer amplifier assumed to have infinite input impedance.

plete amplifier at frequencies between approximately 3.3×10^3 and 10^8 radians per second. As we shall see, the minor-loop feedback mechanism that dominates amplifier performance in this case can be used to advantage for compensation of more complex amplifiers that share the topology of this circuit.

Most modern high-performance operational amplifiers represent relatively straightforward extensions of the circuit shown in Fig. 8.8, and this popularity is a direct consequence of the excellent dynamics associated with the topology. An important modification included in most designs is the use of a more complex second stage than the simple common-emitter amplifier shown in Fig. 8.8 in order to achieve higher d-c open-loop gain. Other options exist in the way the output buffer circuit is realized and the drift-reducing modifications that may be incorporated into the first and second stages.

8.3 HIGH-GAIN STAGES

As mentioned in the previous section, a high-gain second stage is usually used to provide the basic amplifier with the voltage gain normally required

from an operational amplifier. As we shall see, high current gain or high power gain alone is insufficient. It is necessary to have stages with high voltage gain, high transresistance (ratio of incremental output voltage to incremental input current), or both included in an operational-amplifier circuit. Note that there is no restriction on the number of transistors used in the stage. The implication in our definition of stage is that its dynamics are similar to that of a single common-emitter amplifier, that is, it introduces only one pole at frequencies that are low compared to the f_T of the devices used.

Use of the usual hybrid-pi model for the analysis of the simple common-emitter amplifier of Fig. 8.10 shows that the low-frequency incremental voltage is $v_o/v_i = -g_m R_L$ and the incremental transistance is $v_o/i_i = -\beta R_L$. The magnitude of either of these quantities can be increased (seemingly without limit) by increasing R_L. In order to obtain high gains without high supply voltages [the voltage gain of the circuit of Fig. 8.10 is $(q/kT)(V_C - V_O) \simeq 40(V_C - V_O)$], a current source can be used as the collector load. We realize that this technique will not result in infinite voltage gain and transresistance in an actual circuit because the simplified hybrid-pi model does not accurately predict the behavior of circuits with voltage gains in excess of several hundred. In order to proceed it is necessary to develop a more complete hybrid-pi model.

8.3.1 A Detailed Low-Frequency Hybrid-Pi Model[5]

The simplified hybrid-pi model predicts that both the base current and the collector current of a transistor are independent of changes in collector-to-base voltage. Actually, both currents are voltage-level dependent because of an effect called *base-width modulation*, as illustrated by the following argument. Consider an NPN transistor operating at moderate current levels with fixed base-to-emitter voltage V_{BE} and collector-to-base voltage V_{CB}. The approximate charge distribution in the base region for this transistor is shown by the solid line in Fig. 8.11. In this figure, n_p is the minority-carrier concentration in the base region; N_{po} is the equilibrium concentration of electrons in the base region; and x is the distance into the base region with $x = 0$ at the base edge of the emitter-base space-charge layer. The charge distribution drops linearly from its value $n_p(0)$ at $x = 0$ to essentially zero (if the collector-to-base junction is reverse biased by at least several hundred millivolts) at the edge of the collector space-charge layer. However, the width of the collector space-charge layer is

[5] This material is covered in greater detail in P. E. Gray et al., *Physical Electronics and Circuit Models for Transistors*, Wiley, New York, 1964, Chapter 8, and C. L. Searle et al., *Elementary Circuit Properties of Transistors*, Wiley, New York, 1964, Chapter 4.

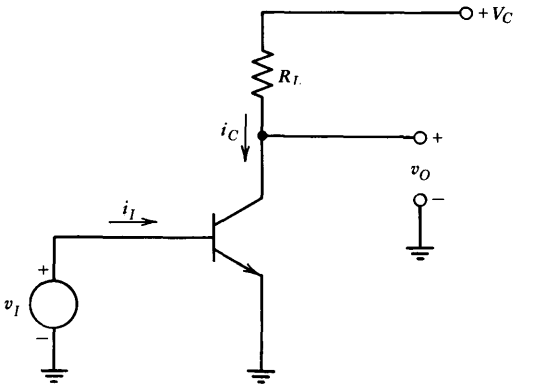

Figure 8.10 Common-emitter amplifier.

monotonically increasing function of collector-to-base voltage. Thus, if the collector-to-base voltage is reduced, the collector space-charge layer becomes narrower. This narrowing increases the effective width of the base region from its original value of W to a new value $W + \Delta W$. The resultant new charge distribution is shown by the dotted line in Fig. 8.11.

Two changes in terminal variables result from this change in base width. First, the collector current (proportional to the slope of the distribution) becomes smaller. Second, the base current increases, since the total rate at which charge recombines in the base region is directly proportional to the total charge in this region. The magnitudes of these changes are calculated as follows.

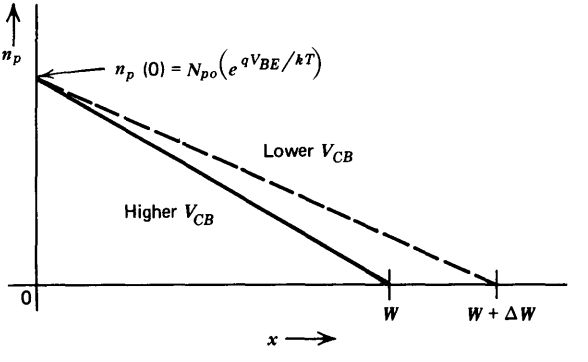

Figure 8.11 Effect of collector-to-base voltage on base-charge distribution (NPN transistor).

The collector current of an NPN transistor is related to transistor and physical constants by

$$I_C = \frac{qN_{po}AD_e}{W} e^{qV_{BE}/kT} \tag{8.13}$$

where

N_{po} is the equilibrium concentration of electrons in the base region.
A is the cross-sectional area of the base.
D_e is the diffusion constant for electrons in the base region.

The assumptions necessary to derive this relationship include operation under conditions of low-level injection but at current levels large compared to leakage currents, and that the ohmic drops in the base region are negligible. The assumption of negligible ohmic voltage drop in the base region results in no loss of generality, since a base resistance can be added to the model which evolves from Eqn. 8.13.

Under conditions of constant base-to-emitter voltage and temperature, Eqn. 8.13 reduces to

$$I_C = \frac{K}{W} \tag{8.14}$$

where the constant K includes all other terms from Eqn. 8.14. Differentiating yields

$$\frac{dI_C}{dW} = -\frac{K}{W^2} \tag{8.15}$$

Differential changes in W are related to incremental changes in collector-to-base voltage as

$$\Delta W = \frac{dW}{dV_{CB}} v_{cb} \tag{8.16}$$

Incremental changes in collector current can thus be expressed in terms of incremental changes in collector-to-base voltage as

$$i_c = -\frac{K}{W^2}\frac{dW}{dV_{CB}} v_{cb} \tag{8.17}$$

Solving Eqn. 8.14 for K and substituting into Eqn. 8.17 yields

$$i_c = -\frac{I_C}{W}\frac{dW}{dV_{CB}} v_{cb} \tag{8.18}$$

The transconductance of a transistor is related to quiescent collector current as

$$g_m = \frac{qI_C}{kT} \tag{8.19}$$

Solving Eqn. 8.19 for I_C and substituting this result into Eqn. 8.18 shows that

$$i_c = \left[- \frac{kT}{qW} \frac{dW}{dV_{CB}} \right] g_m v_{cb} \tag{8.20}$$

The bracketed quantity in Eqn. 8.20 is called the *base-width modulation factor* and is denoted by the symbol η. Introducing this notation and adding the familiar relationship between incremental components of collector current and base-to-emitter voltage to Eqn. 8.20 yields

$$i_c = g_m v_{be} + \eta g_m v_{cb} \tag{8.21}$$

The quantity η is typically 10^{-3} to 10^{-4}, indicating that the collector current is much more strongly dependent on base-to-emitter voltage than on collector-to-base voltage. This is, of course, the reason we are able to ignore the effect of collector-to-base voltage variations except in high-gain situations.

The change in base current as a function of collector-to-base voltage can be calculated with the aid of Fig. 8.11. If reverse injection from the base into the emitter region is assumed small, the base current is directly proportional to the area of the triangle, since the total number of minority carriers that recombine per unit time and thus contribute to base current is proportional to the total number of these carriers in the base region. The geometry of Fig. 8.11 shows that the magnitude of the fractional change in the area of the triangle is equal to the magnitude of the fractional change in slope of the distribution for small changes in W. Furthermore, an increase in W decreases collector current and increases base current. Equating fractional changes yields

$$\frac{i_b}{I_B} = - \frac{i_c}{I_C} = - \frac{\eta g_m v_{cb}}{I_C} \tag{8.22}$$

Rearranging Eqn. 8.22 and recognizing that $I_C/I_B = \beta$ yields for the incremental dependence of base current on collector-to-base voltage at constant base-to-emitter voltage

$$i_b = - \frac{\eta g_m v_{cb}}{\beta} \tag{8.23}$$

Adding the incremental relationship between base current and base-to-emitter voltage to Eqn. 8.23 results in

$$i_b = \frac{g_m}{\beta} v_{be} - \frac{\eta g_m}{\beta} v_{cb} \tag{8.24}$$

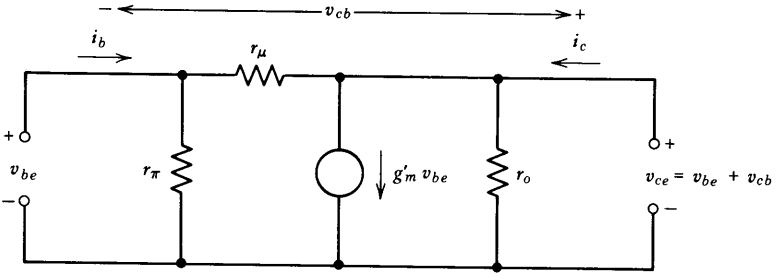

Figure 8.12 Intrinsic hybrid-pi model that includes base-width modulation effects.

It is necessary to augment the familiar hybrid-pi transistor model to include the effects of base-width modulation when the model is used for the analysis of high-gain circuits. While there are several model modifications that would accurately represent base-width-modulation phenomena, convention dictates that the model be augmented by the addition of a collector-to-emitter resistor r_o and a collector-to-base resistor r_μ as shown in Fig. 8.12. The objective is to choose the four elements of the model so that the terminal relationships dictated by Eqns. 8.21 and 8.24 are obtained. Note that, since four degrees of freedom are required to match arbitrary two-port relationships, it may be necessary to have the dependent current-generator scale factor in Fig. 8.12 differ from g_m, and this possibility is indicated by calling this scale factor g'_m.

The terminal relationships developed from the analysis of the effects of base-width modulation are repeated here for convenience:

$$i_c = g_m v_{be} + \eta g_m v_{cb} \tag{8.21}$$

$$i_b = \frac{g_m}{\beta} v_{be} - \frac{\eta g_m}{\beta} v_{cb} \tag{8.24}$$

The equations relating the same variables for the model of Fig. 8.12 are[6]

$$\begin{aligned} i_c &= g'_m v_{be} + g_\mu v_{cb} + g_o(v_{be} + v_{cb}) \\ &= (g'_m + g_o)v_{be} + (g_o + g_\mu)v_{cb} \end{aligned} \tag{8.25}$$

$$i_b = g_\pi v_{be} - g_\mu v_{cb} \tag{8.26}$$

Equationing coefficients in these two sets of equations yields

$$g'_m + g_o = g_m \tag{8.27}$$

[6] Recall that corresponding r's and g's are reciprocally related. Thus, for example, $g_o = 1/r_o$.

$$g_o + g_\mu = \eta g_m \tag{8.28}$$

$$g_\pi = \frac{g_m}{\beta} \tag{8.29}$$

$$g_\mu = \frac{\eta g_m}{\beta} \tag{8.30}$$

These equations are readily solved to determine model element values:

$$g'_m = g_m \left[1 - \eta \left(1 - \frac{1}{\beta}\right)\right] \tag{8.31}$$

$$r_\pi = \frac{1}{g_\pi} = \frac{\beta}{g_m} \tag{8.32}$$

$$r_o = \frac{1}{g_o} = \frac{1}{\eta g_m[1 - (1/\beta)]} \tag{8.33}$$

$$r_\mu = \frac{1}{g_\mu} = \frac{\beta}{\eta g_m} \tag{8.34}$$

Since for any well-designed transistor $|\eta| \ll 1$ (typical values are 10^{-3} to 10^{-4}) and $\beta \gg 1$, the approximations

$$g'_m \simeq g_m = \frac{q|I_C|}{kT} \tag{8.35}$$

and

$$r_o \simeq \frac{1}{\eta g_m} \tag{8.36}$$

usually replace Eqns. 8.31 and 8.33, respectively.

It is instructive to examine the relative magnitudes of the model parameters for a transistor under typical conditions of operation. Assume that a transistor with $\beta = 200$ and $\eta = 4 \times 10^{-4}$ is operated at $I_C = 1$ mA at room temperature. Then $g_m = 40$ mmho, $g_\pi = 200$ μmho or $r_\pi = 5$ kΩ, $g_o = 16$ μmho or $r_o = 62.5$ kΩ and $g_\mu = 0.08$ μmho or $r_\mu = 12.5$ MΩ. Note that all conductances in the intrinsic model are proportional to g_m and therefore to quiescent collector current.

8.3.2 Common-Emitter Stage with Current-Source Load

In spite of the internal loading of r_o and r_μ, high voltage gain is possible with a current-source load for a common-emitter stage, and this connection is used in many operational-amplifier designs. Figure 8.13*a* shows a sche-

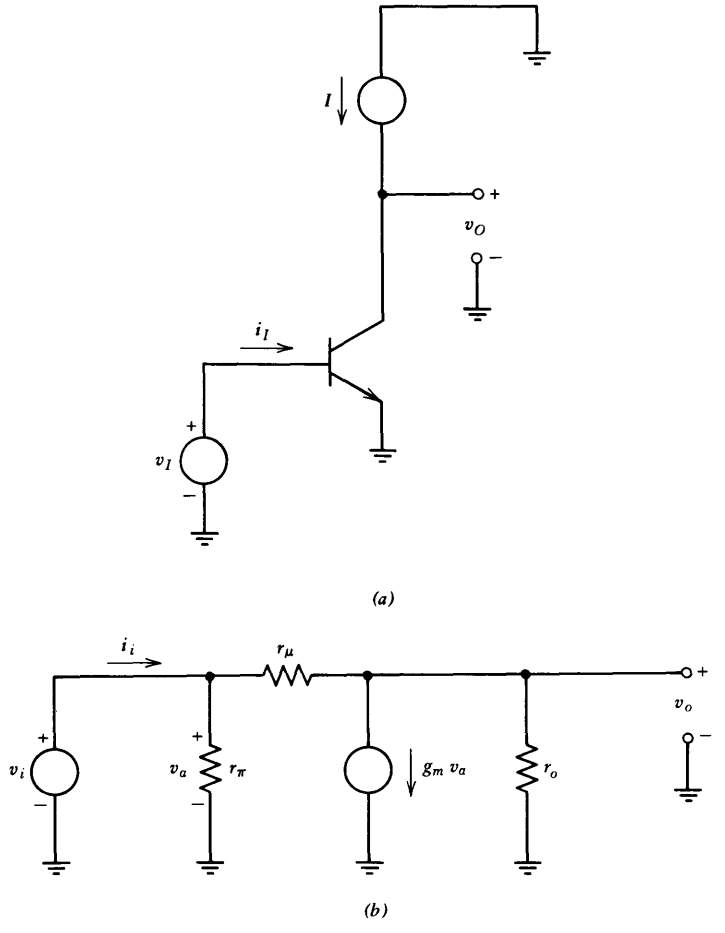

Figure 8.13 Current-source-loaded common-emitter stage. (*a*) Schematic. (*b*) Incremental equivalent circuit (r_x negligibly small).

matic for such a stage and Fig. 8.13*b* is the corresponding low-frequency equivalent circuit. It is assumed that the incremental resistance of the current source is infinite. (The problems associated with realizing a high-resistance current source will be described in Section 8.3.5.) It is also assumed that the base resistance of the transistor can be neglected. This assumption is best justified by considering a complete amplifier where the resistances at various nodes are known. In most anticipated applications r_x will either be small enough so that it can be neglected even for voltage-source drives at the base of the transistor in question, or the value of r_x will be masked by a large driving resistance connected in series with it.

The equivalent circuit of Fig. 8.13*b* is easily analyzed by solving the output-node equation:

$$g_m v_i + g_o v_o + g_\mu(v_o - v_i) = 0 \tag{8.37}$$

Since $g_\mu \ll g_o$ (see Eqns. 8.34 and 8.36) and $g_\mu \ll g_m$,

$$\frac{v_o}{v_i} \simeq -g_m r_o \tag{8.38}$$

With the equivalence of Eqn. 8.36, $r_o = 1/\eta g_m$, the voltage-gain of the circuit becomes simply $-1/\eta$. As mentioned earlier typical values for η are 10^{-3} to 10^{-4}, and therefore a voltage-gain magnitude of 10^3 to 10^4 is possible.

The incremental input current can be calculated as follows.

$$i_i = (g_\pi + g_\mu)v_i - g_\mu v_o \tag{8.39}$$

Substituting from Eqn. 8.38 yields

$$i_i = (g_\pi + g_\mu + g_m r_o g_\mu)v_i \tag{8.40}$$

Recognizing that

$$g_m r_o g_\mu = g_\pi \tag{8.41}$$

simplifies Eqn. 8.40 to

$$i_i = (2g_\pi + g_\mu)v_i \simeq 2g_\pi v_i \tag{8.42}$$

This relationship indicates that the use of a current-source load halves the input resistance of a common-emitter amplifier compared to the value when loaded with a moderate-value resistor, since the currents flowing through r_π and r_μ are equal in this high-gain connection.

Combining Eqns. 8.42 and 8.38 shows that the transresistance is

$$\frac{v_o}{i_i} = -\frac{r_\pi g_m r_o}{2} = -\frac{\beta r_o}{2} = -\frac{r_\mu}{2} \tag{8.43}$$

The dominant pole for this amplifier, at least for realistic values of driving-source resistance, occurs at the input. Because of the high voltage gain, the input capacitance includes a component several thousand times larger than C_μ, and this effective input capacitance is the primary energy-storage element.

8.3.3 Emitter-Follower Common-Emitter Cascade

The current-source-loaded common-emitter stage analyzed in the preceding section can be driven with an emitter follower to increase transresistance. Figure 8.14 illustrates this connection. Analysis is simplified by applying the results of the last section. Since the input resistance of the

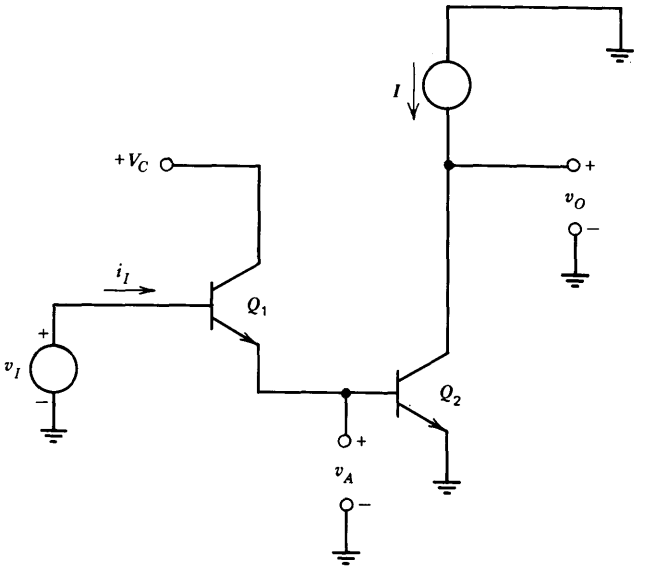

Figure 8.14 Emitter-follower common-emitter cascade.

common-emitter amplifier is $r_\pi/2$ (Eqn. 8.42), the transfer ratios v_a/v_i and v_a/i_i can be calculated by replacing the input circuit of Q_2 with a resistor equal to $r_{\pi 2}/2$. These results are combined with Eqns. 8.38 and 8.42 to determine gain and transresistance. Furthermore, it is not necessary to consider elements r_o and r_μ in the model for transistor Q_1 since the voltage gain of this device is low. An incremental equivalent circuit that relates v_a to v_i is shown in Fig. 8.15.

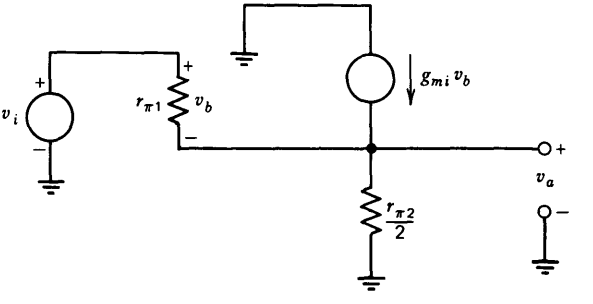

Figure 8.15 Equivalent circuit used to determine v_a/v_i for circuit of Fig. 8.14.

The voltage-transfer ratio is

$$\frac{v_a}{v_i} = 1 - \frac{1}{1 + r_{\pi 2}/2r_{\pi 1} + g_{m1}r_{\pi 2}/2} \tag{8.44}$$

For the circuit of Fig. 8.14 the quiescent collector current of Q_2 is I, while that of Q_1 is approximately I/β_2. Therefore,

$$r_{\pi 2} = \frac{\beta_2}{g_{m2}} = \frac{\beta_2 kT}{qI} \tag{8.45}$$

and

$$r_{\pi 1} = \frac{\beta_1}{g_{m1}} = \frac{\beta_1\beta_2 kT}{qI} = \beta_1 r_{\pi 2} \tag{8.46}$$

Equation 8.46 shows that for reasonable values of β_1, the term $r_{\pi 2}/2r_{\pi 1}$ in Eqn. 8.44 can be dropped.

Introducing this simplification and noting that $g_{m2} = \beta_2 g_{m1}$, so that $r_{\pi 2} = 1/g_{m1}$ reduces Eqn. 8.44 to

$$\frac{v_a}{v_i} = \frac{1}{3} \tag{8.47}$$

Therefore

$$\frac{v_o}{v_i} = -\frac{1}{3\eta_2} \tag{8.48}$$

Since $v_a = \frac{1}{3} v_i$, the input resistance is

$$\frac{v_i}{i_i} = \frac{3}{2} r_{\pi 1} \tag{8.49}$$

Combining Eqns. 8.48 and 8.49 shows that the transresistance is

$$\frac{v_o}{i_i} = -\frac{r_{\pi 1}}{2\eta_2} \tag{8.50}$$

This equation can be compared with Eqn. 8.43 by noting that $r_{\pi 1} = \beta_1\beta_2/g_{m2}$. Thus

$$\frac{v_o}{i_i} = -\frac{\beta_1\beta_2}{2g_{m2}\eta_2} = -\frac{\beta_1 r_{\mu 2}}{2} \tag{8.51}$$

Transistor Q_1 simply improves the transresistance of the circuit by a factor of β_1.

The dominant pole for this circuit is associated with the input of Q_2, since the incremental resistance to ground at this point remains high even with the emitter follower included.

8.3.4 Current-Source-Loaded Cascode

The gain limitations of the common-emitter amplifier stem from an internal negative-feedback mechanism related to transistor operation. As the collector-to-base voltage changes, the effective width of the base region also changes and resulting variations in collector- and base-terminal current oppose the original change. This effect is similar to that of the collector-to-base capacitance C_μ that supplies charge to both the collector and base terminals in such a direction as to oppose rapid variations in collector voltage. The cascode connection, which is useful because it minimizes feedback through C_μ at high frequencies, can also be used to minimize the effects of base-width modulation on circuit performance.

A connection that combines a cascode amplifier with a current-source load is shown in Fig. 8.16. This circuit can be analyzed by brute-force techniques, or a little thought can be traded for a page of calculations. We have already shown that the voltage gain of a current-source-loaded common-emitter amplifier is $-1/\eta$.

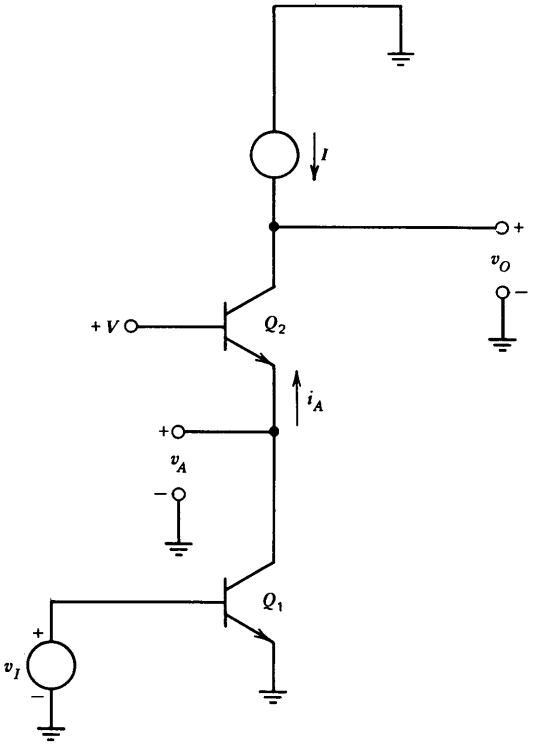

Figure 8.16 Cascode amplifier with current-source load.

Therefore the transfer ratio v_o/v_a in Fig. 8.16 is

$$\frac{v_o}{v_a} = \frac{1}{\eta_2} + 1 \simeq \frac{1}{\eta_2} \tag{8.52}$$

We have also shown that the input resistance for the common-emitter amplifier is $r_\pi/2$. Observe that since the incremental collector current of Q_2 cannot change in the connection of Fig. 8.16, the incremental ratio v_a/i_a must be the same as the input resistance of the common-emitter amplifier, or

$$\frac{v_a}{i_a} = \frac{r_{\pi 2}}{2} \tag{8.53}$$

The voltage gain of Q_1 can be calculated by simply assuming it is loaded with a resistor equal $r_{\pi 2}/2$. Accordingly,

$$\frac{v_a}{v_i} = -g_{m1}\frac{r_{\pi 2}}{2} \tag{8.54}$$

providing this gain is small enough so that $r_{\mu 1}$ and r_{o1} are negligible. Equation 8.54 can be simplified by noting that $r_{\pi 2} = \beta_2/g_{m2}$, and that $g_{m1} = g_{m2}$ since both devices are operating at virtually identical quiescent currents. With this relationship the voltage gain of the current-source-loaded cascode becomes

$$\frac{v_o}{v_i} = -\frac{\beta_2}{2\eta_2} \tag{8.55}$$

Since the input resistance of Q_1 is $r_{\pi 1}$, the transresistance for the circuit is

$$\frac{v_o}{i_i} = -\frac{\beta_2 r_{\pi 1}}{2\eta_2} = -\frac{\beta_2\beta_1}{2\eta_2 g_{m1}} = -\frac{\beta_2\beta_1}{2\eta_2 g_{m2}} = -\frac{\beta_1 r_{\mu 2}}{2} \tag{8.56}$$

Comparing the cascode with the two previous circuits, we see that it provides the same transresistance as the circuit including the emitter follower and has significantly higher voltage gain than either of the other circuits. It is of practical interest to note that transistors are available that can provide voltage gains in excess of 10^5 in this connection.

The dominant pole occurs at the collector of Q_2 because the incremental resistance at this node is extremely high. The use of the cascode reduces the capacitance seen at the base of Q_1 so that even with a high source resistance, the time constant at this node is typically between 100 and 10,000 times shorter than the collector-circuit time constant.

8.3.5 Related Considerations

The circuits described in the last three sections offer at least one further advantage that is useful for the design of operational amplifiers. The cur-

rent source included in all of these circuits insures that the transistors operate at quiescent current levels that are essentially independent of output voltage. Large output-voltage swings are therefore possible without altering any current-dependent transistor parameters.

Care may be required in the design of a current source with sufficiently high output resistance to prevent significant loading of the high-gain stages. Figure 8.17*a* shows a transistor connected as a current source. The output resistance for this connection determined from the incremental circuit model is

$$\frac{v_o}{i_o} = r_\mu \left\| \left[\frac{1 + (g_m + g_o)(r_\pi \| R_E)}{g_o} \right] \simeq r_\mu \right\| \left[\frac{1 + g_m(r_\pi \| R_E)}{g_o} \right] \tag{8.57}$$

The output resistance varies from

$$\frac{v_o}{i_o} \simeq r_o \qquad \text{for} \qquad R_E = 0 \tag{8.58}$$

to

$$\frac{v_o}{i_o} \simeq r_\mu \left\| \frac{g_m r_\pi}{g_o} = \frac{r_\mu}{2} \right. \qquad \text{for} \qquad R_E \gg r_\pi \tag{8.59}$$

This analysis indicates that it is not possible to build a current source of this type with an output resistance in excess of $r_\mu/2$.

Since r_μ is current dependent and since the current source operates at a current level equal to that of its driving transistor in the high-gain circuits, r_μ and r_o for a current-source transistor will be comparable to those of the driving transistor. The analysis of Section 8.3.2 can be extended to show that the output resistance of the common-emitter stage is r_o when driven from a voltage source and is $r_o/2$ when driven from a high impedance source. Thus use of a common-emitter current source ($R_E = 0$ in Fig. 8.17) can reduce the gain of this stage by as much as a factor of two. Since the output resistance of the emitter-follower common-emitter cascode is $2r_o/3$ when driven from a voltage source, the susceptibility of this stage to loading is comparable to that of the common-emitter stage.

The output resistance of the cascode is $r_\mu/2$, so even the highest output resistance that can be achieved with a bipolar-transistor current source will halve the unloaded gain of this stage. A further practical difficulty is that approaching a current-source resistance of $r_\mu/2$ requires $R_E \gg r_\pi$ (Eqn. 8.57). If we assume the base-to-emitter voltage of the transistor is small compared to V in Fig. 8.17*a*,

$$R_E \simeq \frac{V}{I_E} = \frac{qV}{kTg_m} \simeq \frac{40Vr_\pi}{\beta} \tag{8.60}$$

In order to satisfy the inequality $R_E \gg r_\pi$, it is necessary to have $V \gg \beta/40$.

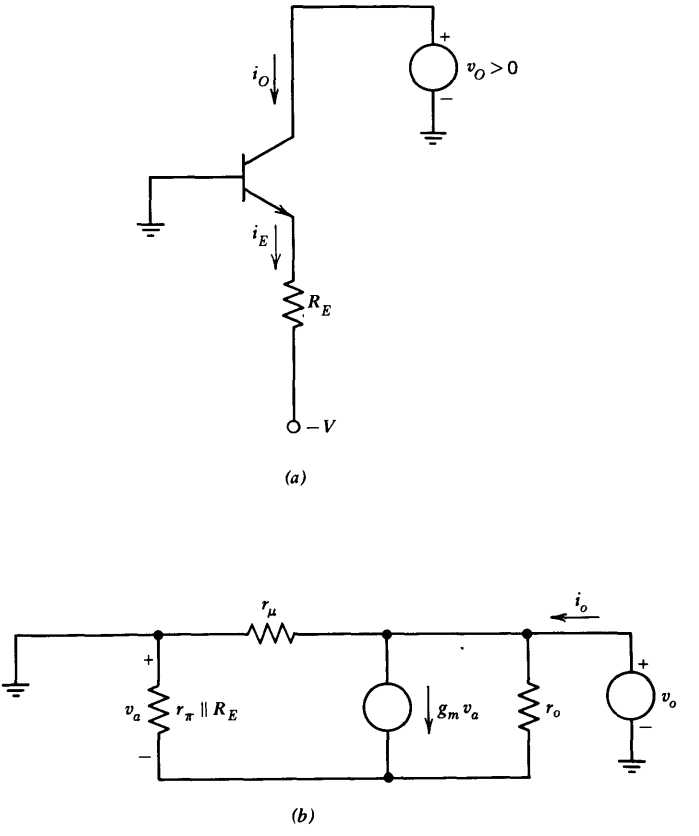

Figure 8.17 Current source. (*a*) Schematic. (*b*) Equivalent circuit.

The use of low β transistors is not the answer, since such transistors also have low r_μ. One way to avoid the requirement for high supply voltage is to use the connection of Fig. 8.18. Cascoding serves the same function as it does in the amplifier, and provides an output resistance of approximately $r_\mu/2$ with a total supply voltage of several volts.

The analysis presented above shows that the output resistance of a bipolar-transistor current source is bounded by $r_\mu/2$, and that this maximum value occurs only when the base of the transistor is connected to a low resistance level relative to the emitter-circuit resistance. Field-effect transistors (FET's) can be used in the interesting connection shown in Fig. 8.19*a* to increase the output resistance of a current source. A model that can be used for the linear-region analysis of the FET is shown in Fig. 8.19*b*. An incremental equivalent circuit of the cascoded source, assuming that the finite output resistance of the current source $R_S = v_a/i_a$ completely de-

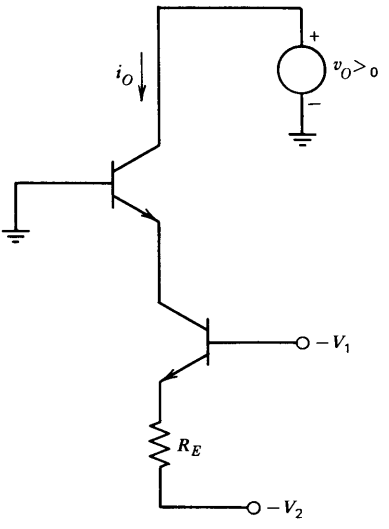

Figure 8.18 Cascoded current source.

scribes this element, is shown in Fig. 8.19*c*. This equivalent circuit shows that the relationship between v_o and i_o is

$$v_o = i_o R_S + \frac{i_o}{y_{os}} + \frac{i_o R_S y_{fs}}{y_{os}} \tag{8.61}$$

or that

$$\frac{v_o}{i_o} = \frac{1}{y_{os}} + R_S\left(1 + \frac{y_{fs}}{y_{os}}\right) \tag{8.62}$$

Since the quantity y_{fs}/y_{os} can be several hundred or more for certain FET's, this connection greatly increases the incremental resistance of the current source itself. For example, by using a bipolar-transistor current source cascoded with a FET, incremental resistances in excess of 10^{12} Ω can be obtained at a quiescent current of 10 μA. It is theoretically possible to further increase current-source output resistance by using multiple cascoding with FET's, although stray conductance limits the ultimate value in actual circuits.

Another problem that occurs in the design of high-gain stages is that the output of the stage must be isolated with a very high-input-resistance buffer to prevent loading that can cause a severe reduction in the voltage gain of the stage. One approach is to use a FET as a source follower, since the input resistance of this connection is essentially infinite. The use of a FET as a buffer or to cascode a current source is frequently the best technique

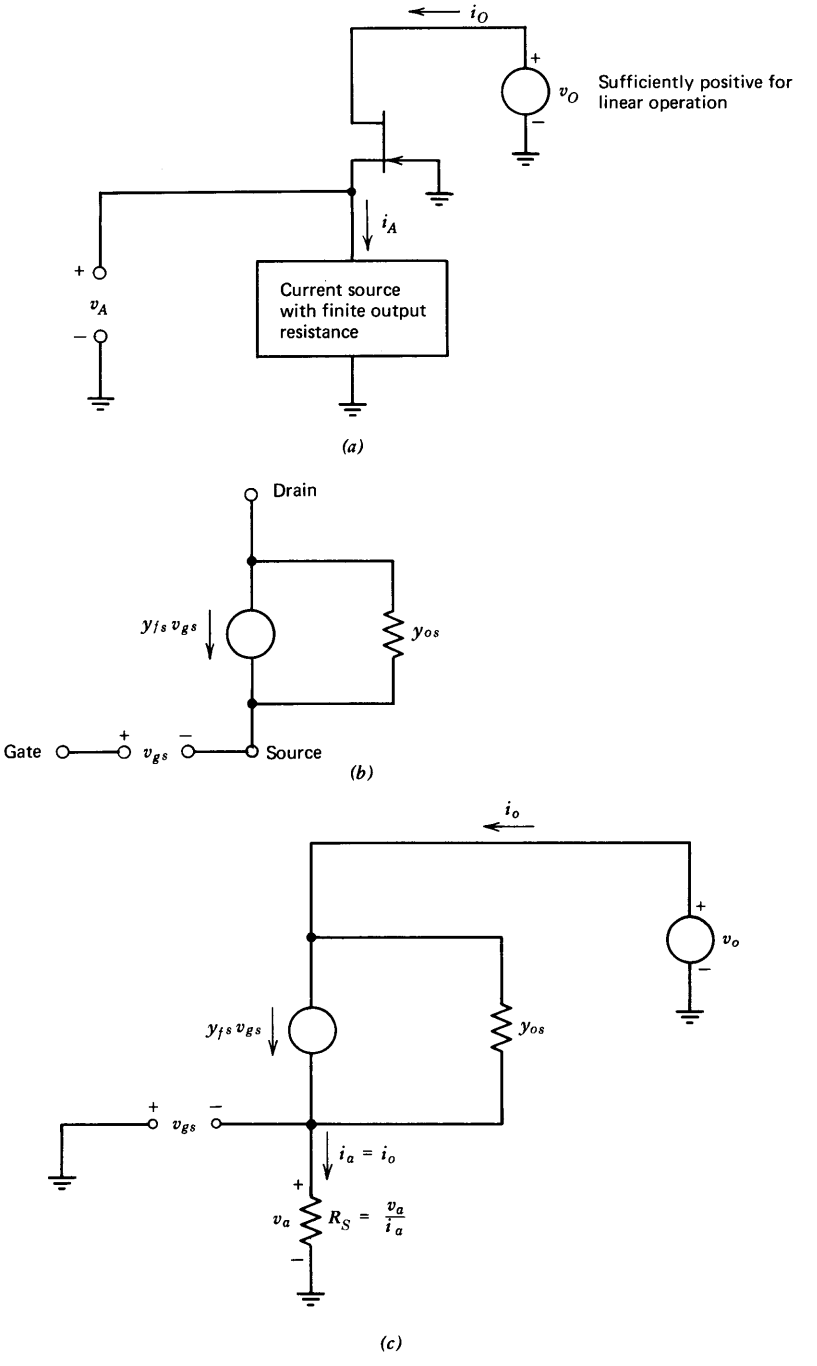

Figure 8.19 Current source cascoded with a field-effect transistor. (*a*) Circuit. (*b*) Linear model for field-effect transistor. (*c*) Incremental equivalent circuit.

in discrete-component designs. However, it is presently difficult to fabricate high-quality bipolar and field-effect transistors simultaneously in monolithic integrated-circuit designs; thus alternatives are necessary for these circuits.

If a bipolar-transistor emitter follower (Fig. 8.20) is used, care must be taken to insure sufficiently high input resistance. The incremental input resistance for this circuit with no additional loading is

$$\frac{v_i}{i_i} \simeq r_\mu \| [r_\pi + \beta(r_o \| R_E)] \tag{8.63}$$

In order to approach the maximum input resistance of $r_\mu/2$ (particularly important if the buffer is to be used with the cascode amplifier), it is necessary to have $R_E \gg r_o$. This inequality normally cannot be satisfied with reasonable supply voltages, so a current source is frequently used in place of R_E. A further advantage of the current source is that the drive current that can be supplied to any following stage becomes independent of voltage level.

One design constraint for an emitter follower intended for use with the current-source-loaded cascode amplifier is that the quiescent operating current of this stage should not be large compared with that of the cascode or else the gain of the stage will be determined primarily by r_μ of the emitter follower.

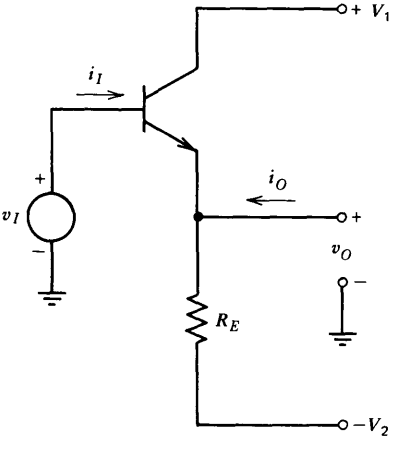

Figure 8.20 Emitter follower.

8.4 OUTPUT AMPLIFIERS

Factors that influence the design of the differential amplifier normally used as the input stage of an operational amplifier were investigated in Chapter 7, and the design of stages that provide high voltage gain was covered in earlier sections of this chapter. Modern operational amplifiers that combine a differential-amplifier input stage (often current-source loaded) with a current-source-loaded second stage require a final amplifier to supply output current and to provide additional isolation for the preceding high-gain stage. The dividing line between the devices used primarily to supply output current and those used to isolate the high-resistance node of the high-gain stage is often hazy. The emphasis in this section is on the power-handling aspect of the output amplifier. The guidelines of the previous section are used when isolation is the major objective.

Some type of emitter-follower circuit is almost always used as the output stage of an operational amplifier, since this configuration combines the necessary current gain with dynamics that can usually be ignored until frequencies above the unity-gain frequency of the complete amplifier are reached.

The simplest emitter-follower connection is shown in Fig. 8.21, and this circuit is powered from the ± 15-volt supplies that have become relatively standard for operational amplifiers. While this circuit can provide the necessary output current and isolation, it requires high quiescent power relative to the maximum power it can supply to the load. If the circuit is designed so that the output voltage can swing to at least -10 volts (a typical value

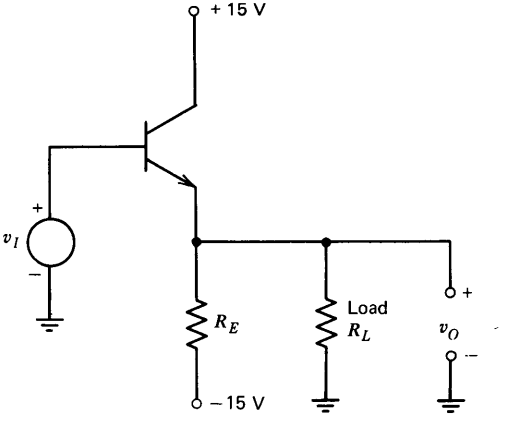

Figure 8.21 Emitter follower with resistive biasing.

for operation from 15-volt supplies), it is necessary to make R_E equal to half the minimum expected load resistance, since at the most negative output voltage the transistor will be cut off and the load current must be supplied via R_E. If, for example, $R_L = 500\ \Omega$, R_E must be less than or equal to 250 Ω to insure that a -10-volt output level can be obtained. The power delivered to the load is 200 mW at $v_O = \pm 10$ volts, while the total power required from the supplies under quiescent conditions ($v_O = 0$) is 1.8 watts, or power nine times as large as the maximum output power for negative output voltage. This low ratio of peak output power to quiescent power is intolerable in many applications. A second and related problem is that the input resistance to the stage will be only $\beta R_L/3$ when R_E is selected to guarantee a -10-volt output.

The situation improves significantly if the biasing resistor is replaced by a current source as shown in Fig. 8.22. A -10-volt output is obtained with $I = 10\ \text{volts}/R_L$. If we use the earlier value of 500 Ω for R_L, a 200-mW peak output for negative output voltage results with 600 mW of quiescent power consumption. The input resistance to the circuit is similarly increased by a factor of three.

Further improvement results if a complementary emitter follower (Fig. 8.23) is used. Neither transistor in this connection is forward biased with $v_I = v_O = 0$, and thus the quiescent power consumption of the circuit is zero. The NPN supplies output current for positive output voltages, while the PNP supplies the current for negative output voltages. In either case only one transistor conducts, so that the load current only is required from the loaded power supply.

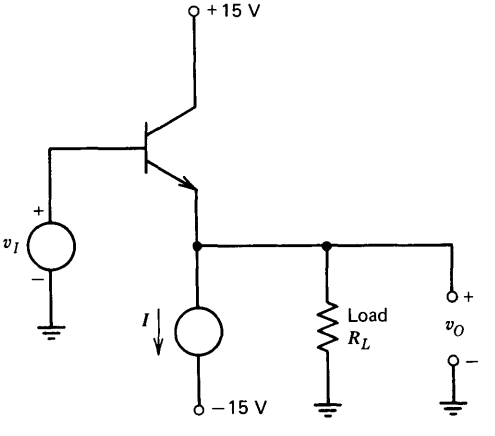

Figure 8.22 Emitter follower with current-source biasing.

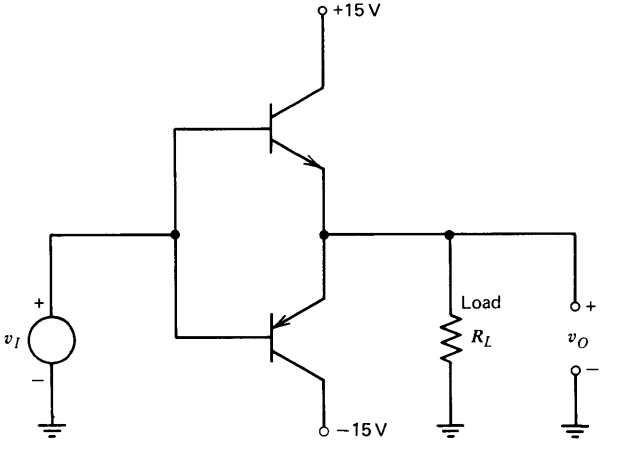

Figure 8.23 Complementary emitter follower.

As might be expected, the complementary emitter follower has its own design problems; the most difficult of these involve establishing appropriate quiescent levels. If the circuit is constructed as shown in Fig. 8.23, it exhibits *crossover distortion* since it is necessary to forward bias either transistor base-to-emitter junction by approximately 0.6 volt to initiate conduction. Consequently, there is a 1.2-volt range of input voltage for which the output remains essentially zero. The idealized transfer characteristics as well as representative input and output waveforms for this circuit are shown in Fig. 8.24. We might initially feel that, since this circuit is intended for use as the output stage of an operational amplifier, the effect of this nonlinearity would be reduced to insignificant levels by the gain that precedes it in most feedback applications. In fact, the example presented in Section 2.3.2 showed that feedback virtually eliminated the distortion from this type of dead zone in one system. Unfortunately, the moderation of the nonlinearity depends on the gain of the linear elements in the loop, and is often insufficient at higher frequencies where this gain is reduced. As a result, while an output stage as simple as the one shown in Fig. 8.23 is at times successfully used in high-power low-frequency applications, it must normally be linearized to yield acceptable performance in moderate- to high-frequency situations.

The required linearization is accomplished by forward biasing the base-to-emitter junctions of the transistors so that both are conducting at low levels with zero input signal. One conceptually possible biasing scheme is shown in Fig. 8.25. If each of the two batteries is selected to just turn on its respective transistor, the input and output voltages of circuit will be identi-

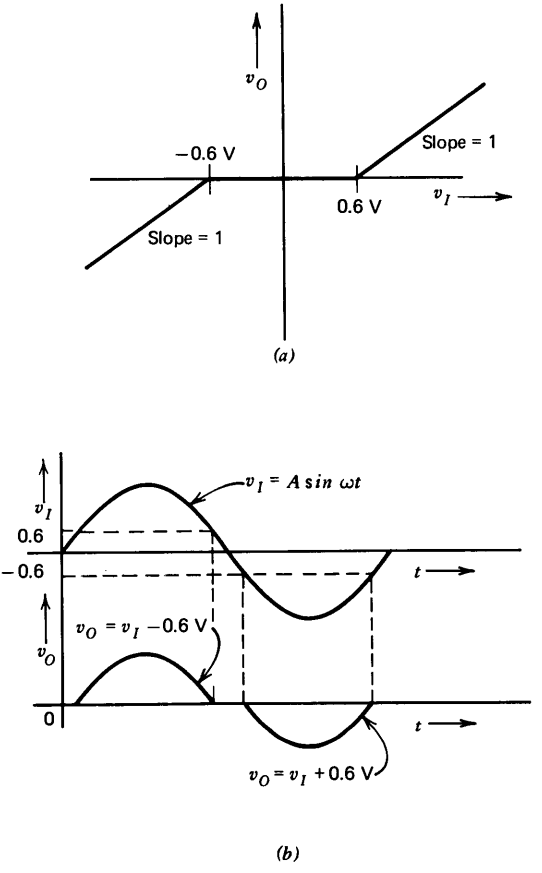

Figure 8.24 Input-output relationships for the complementary emitter follower. (*a*) Transfer characteristics. (*b*) Waveforms.

cal. Ignoring the practical difficulties involved in realizing the floating voltage sources (which can be resolved), two types of difficulties are probable: the biasing voltages will either be too small or too large. These problems occur because of the exponential and highly temperature-dependent relationship between collector current and base-to-emitter voltage. If too small bias voltages are used, a fraction of the crossover distortion remains, while if the bias voltages are too large, the circuit can conduct substantial quiescent current through the two transistors, and there is the probability of *thermal runaway*.

Thermal runaway is a potentially destructive process that is most easily understood by considering a transistor biased with a fixed base-to-emitter

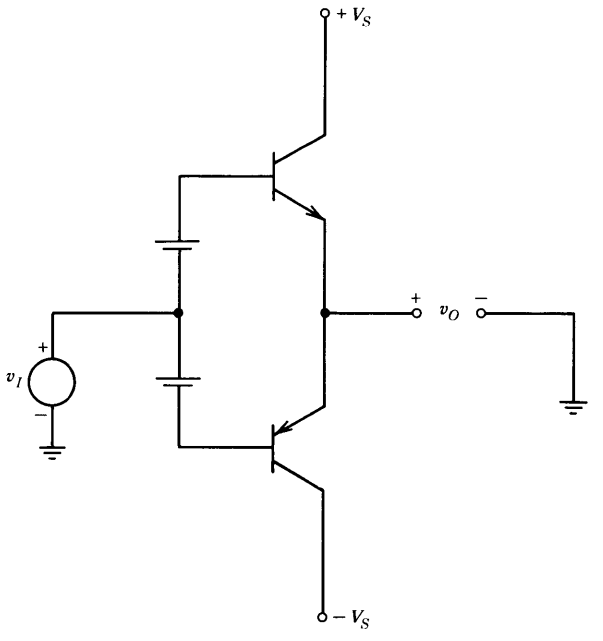

Figure 8.25 One approach to biasing the complementary emitter follower.

voltage so that it conducts some collector current. The power dissipation that results heats the transistor, and since the device is operating at fixed base-to-emitter voltage, the resultant temperature increase leads to a larger collector current, which results in higher power dissipation, etc. If the gain around this thermal positive-feedback loop exceeds one, the collector current increases until the transistor dies. (See Problem P8.13.)

In order to avoid these difficulties, forward-biased junctions are normally used to provide the bias voltages. If these biasing junctions are matched to the output-transistor base-to-emitter junctions and located in close thermal proximity to them, excellent control of bias current results. This approach is particularly attractive for monolithic integrated-circuit designs because of the ease of obtaining matched, isothermal devices with this construction technique. Further insurance against thermal runaway is often obtained by including resistors in series with the emitters of the output transistors. Voltage drops across these resistors reduce base-to-emitter voltage and thus tend to stabilize bias currents as these currents increase. The value of these resistors represents a compromise between the increased operating-point stability that results from higher-value resistors and the lower output re-

sistance associated with smaller resistors. A compromise value of approximately 25 Ω is frequently used for designs with peak output current in the 20-mA range.

One interesting bias-circuit variation for a complementary emitter-follower connection is used in the 741 integrated-circuit operational amplifier. This circuit is shown in simplified form along with quiescent current levels in Fig. 8.26. The circled components function as a diode and a half (or more precisely a diode and three-fifths) to establish a conservative bias-voltage value. Because the base current of the transistor is small compared to the currents through the two resistors, this negative-feedback connection forces the voltages across the resistors to be proportional to their relative values.

While forward-biasing techniques make the use of complementary connections practical, minor nonlinearities usually remain. For this reason, operational amplifiers intended for use at very high frequencies occasionally use a current-source-biased emitter follower (Fig. 8.22) in order to achieve improved linearity.

It is often necessary to incorporate current limiting in the design of an output stage intended for general-purpose applications. While it would be ideal if the current limit protected the amplifier for shorts from the output to ground or either supply voltage, this requirement often severely compromises maximum output current. Consequently, the current limit is at times designed for protection from output-to-ground shorts only.

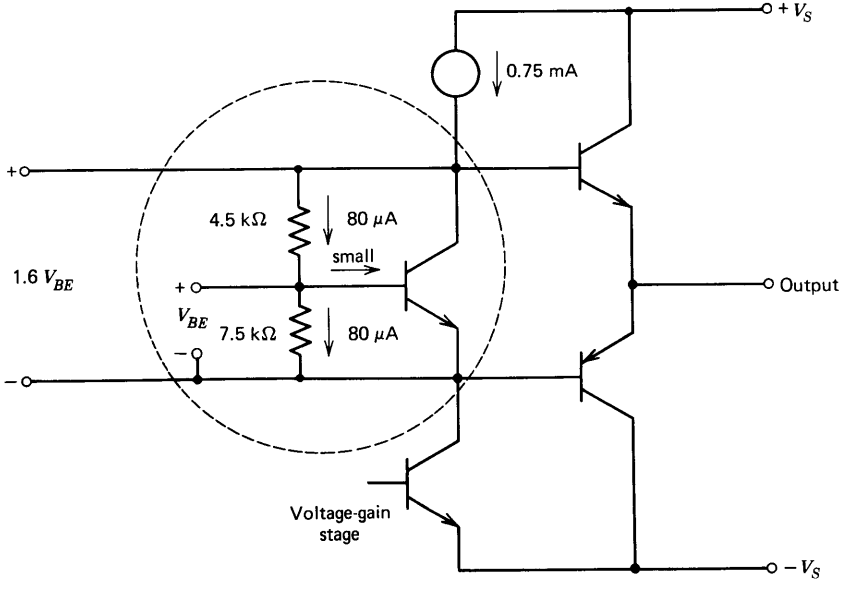

Figure 8.26 Bias circuit used in 741 amplifier.

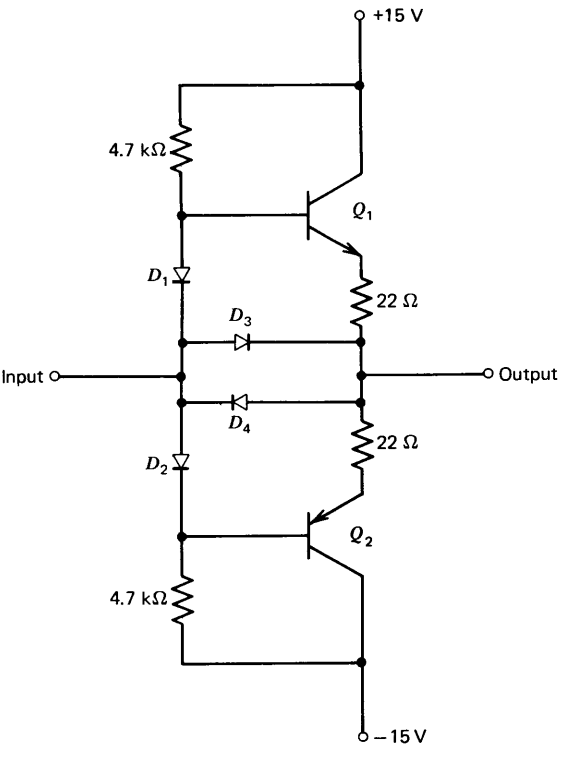

Figure 8.27 Resistively biased complementary emitter follower.

Figure 8.27 shows a discrete-component output stage that illustrates some of the concepts introduced above. Assume that the input and output voltage levels are both zero, and that no current is drawn from the output. Under these conditions, approximately 3 mA flows through diodes D_1 and D_2 and the two 4.7-kΩ resistors. If diodes D_1 and D_2 are matched to the base-to-emitter junctions of Q_1 and Q_2, respectively, the quiescent bias current of the transistor pair is slightly more than 1 mA. (The details of this type of calculation are given in Section 10.3.1.) The 22-Ω resistors effectively protect against thermal runaway. Assume, for example, that the temperatures of the transistor junctions each rise 50° C above their respective diodes. As a result of this temperature differential, the voltage across each 22-Ω resistor increases by at most 100 mV, and thus the quiescent-current increase is limited to less than 5 mA.

Base drive for the transistors is supplied from the 4.7-kΩ resistors rather than directly from the input-signal source. The current limit occurs when this required drive current is eliminated in the following way. Assume that

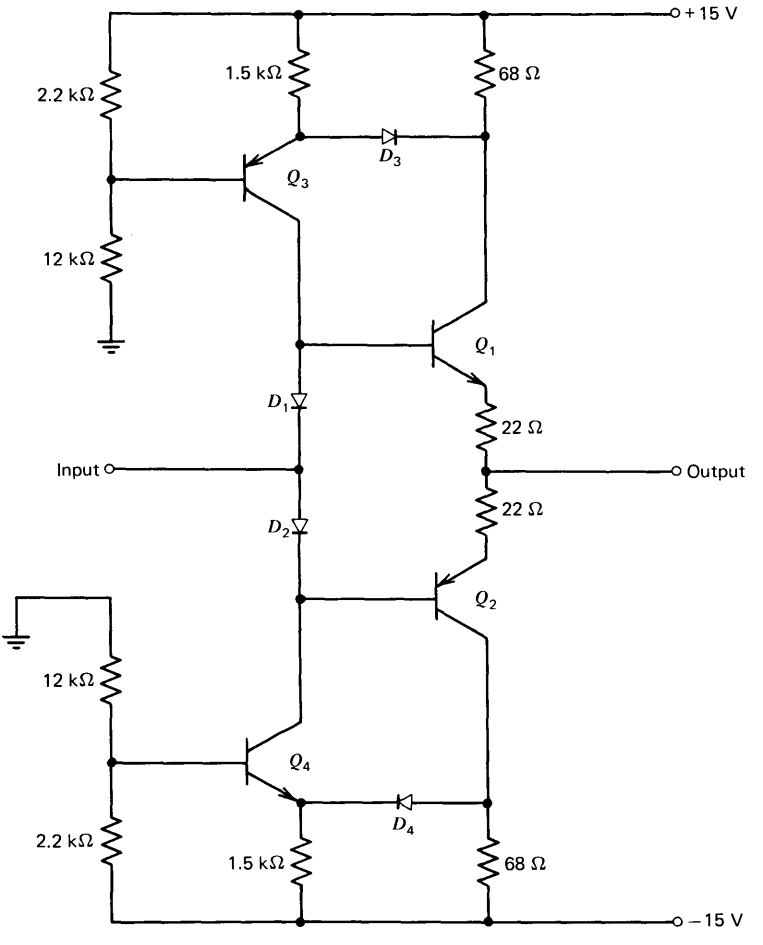

Figure 8.28 Current-source biased complementary emitter follower.

the input voltage is positive and that transistor Q_1 is supplying an output current of approximately 25 mA. Under these conditions diode D_3 is on the verge of conduction, since with approximately the same voltages across D_1 and the base-to-emitter junction of Q_1, the voltages across the top 22-Ω resistor (22 Ω × 25 mA = 550 mV) and D_3 are nearly equal. If the input-signal source is limited to low current output, diode D_3 clamps the input voltage level, preventing further increases in base drive. Because the limiting current level is proportional to the forward voltage of a diode, the limiting level decreases with increasing ambient temperature. This dependence is

advantageous, since the power-handling capacity of the output transistors also decreases with increasing temperature.

This relatively simple circuit is often an adequate output stage. One deficiency is that the input resistance of the circuit is dominated by the parallel combination of the biasing resistors. Since the output current is limited to approximately 25 mA, minimum load resistors on the order of 400 Ω are anticipated. The current gain of the output pair insures that the input loading attributable to this value of load resistor is insignificant compared to that of the biasing resistors. Increasing the value of the biasing resistors can result in insufficient base drive at maximum output voltages.

The circuit shown in Fig. 8.28 can be used when maximum input resistance to the buffer amplifier is required. Diodes D_1 and D_2 function as they did in the previous circuit. However they are biased with 1-mA current sources formed by transistors Q_3 and Q_4 rather than by resistors. The high incremental resistance of these current sources minimizes loading at the amplifier input. Since the current sources supply base drive for the output transistors, turning these current sources off limits output current. The limiting occurs as follows for a positive input voltage. When the output current is approximately 30 mA, the voltage at the cathode end of diode D_3 equals the voltage at the base of Q_3. Further increases in output current lower the upper current-source magnitude, thereby reducing drive.

PROBLEMS

P8.1

Consider an operational amplifier built with n identical stages, and an open-loop transfer function

$$a(s) = \frac{a_o}{(\tau s + 1)^n}$$

This amplifier is used in a noninverting unity-gain connection. Determine the maximum stable value of a_o for $n = 3$ and $n = 4$. What is the limiting stable value for a_o as $n \rightarrow \infty$?

P8.2

Figure 8.29 illustrates a model for a multiple-stage operational amplifier. The output impedance of the input section of the amplifier is very high, and the transfer admittance is

$$y(s) = \frac{I_a(s)}{V_i(s)} = \frac{0.67 \times 10^{-2}}{(10^{-6}s + 1)(10^{-7}s + 1)}$$

The quiescent collector current of the transistor is 100 μA. Transistor parameters include $\beta = 100$, $C_\mu = 5$ pF, and $C_\pi = 10$ pF. You may as-

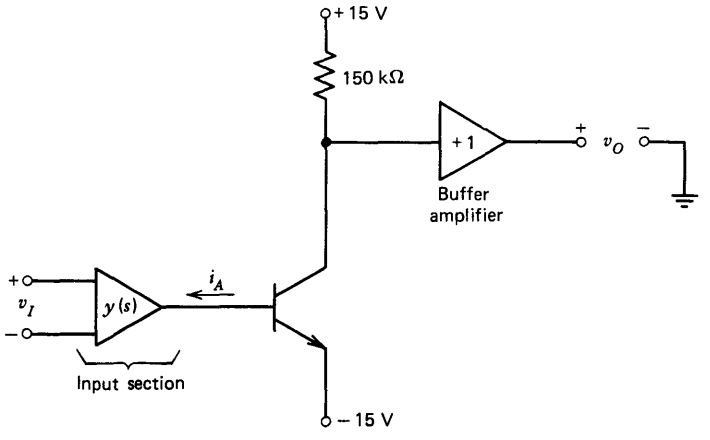

Figure 8.29 Multiple-stage operational amplifier.

sume that a one-pole approximation adequately characterizes the common-emitter stage, and that the input impedance of the buffer amplifier is very high. Ignore base-width-modulation effects.

(a) Find the transfer function $V_o(s)/V_i(s)$ for this amplifier. What is the magnitude of this transfer function at the frequency where it has a phase shift of $-180°$?
(b) Determine a compensating impedance that can be placed between base and emitter of the transistor so that the second pole of the compensated transfer function occurs near its unity-gain frequency. What is the open-loop transfer function with your compensation?
(c) Find a compensating impedance that can be placed between collector and base of the transistor to yield a transfer function similar to that obtained in part *b*.

P8.3

A model for an operational amplifier incorporating feedforward compensation is shown in Fig. 8.30. Approximate the open-loop transfer func-

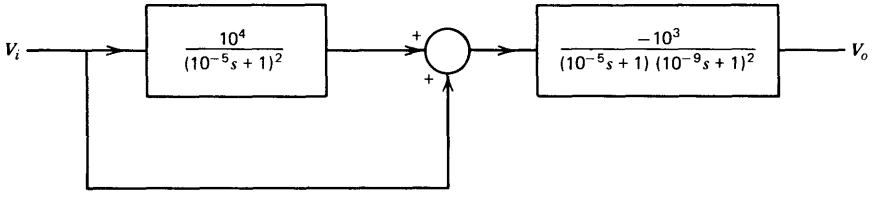

Figure 8.30 Block diagram for feedforward amplifier.

tion $V_o(s)/V_i(s)$ for this amplifier. (Note that you should be able to estimate the transfer function of interest fairly accurately without having to factor any polynomials.) What is the amplifier phase shift at its unity-gain frequency? Draw a Bode plot of the transfer function. Comment on possible difficulties with this amplifier.

P8.4

Do you expect the base-width modulation factor η of a bipolar transistor to be more strongly dependent on quiescent collector current or quiescent collector-to-emitter voltage? Explain.

P8.5

Figure 8.31 shows the characteristics of a certain NPN transistor as displayed on a curve tracer when the base current is 10 μA. Find values for g_m, r_π, r_o, and r_μ for this device valid at $I_C = 1$ mA, $V_{CE} = 10$ volts. Estimate η for this transistor.

P8.6

Assume that the transistor connection shown in Fig. 8.14 is modified to include a bias current source that increases the value of the emitter current of Q_1. Express the voltage gain and transresistance of the resulting circuit in terms of the value of the bias source and other circuit parameters.

P8.7

A current-source-loaded Darlington connection is shown in Fig. 8.32. Find the low-frequency voltage gain and transresistance of this circuit, assuming that both transistors have identical values for β and η.

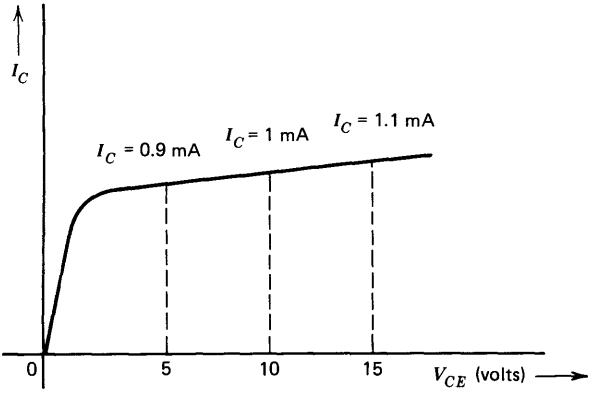

Figure 8.31 Transistor *I-V* characteristics.

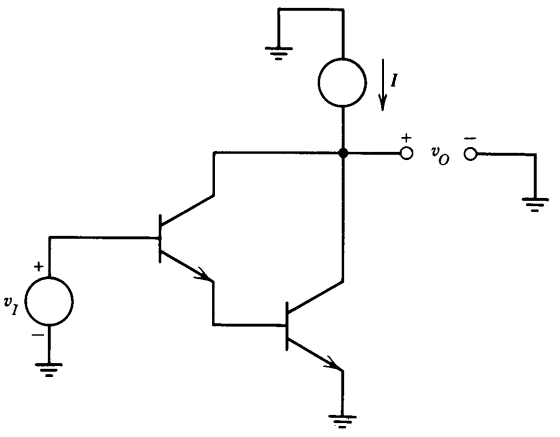

Figure 8.32 Current-source-loaded Darlington amplifier.

P8.8

Determine the low-frequency gain v_o/v_i and transresistance v_o/i_i for the current-source-loaded differential amplifier shown in Fig. 8.33. Assume both transistors are identical and characterized by β and η.

P8.9

A bipolar transistor is used in a current-source connection with its emitter connected to ground. Compare the output resistances that result when the base of the transistor is biased with a high or a low resistance source. Show that the same values result for the output resistance of a common-emitter amplifier loaded with an ideal current source as a function of the driving-source resistance.

P8.10

A transistor is available with $\beta = 200$ and $\eta = 5 \times 10^{-4}$. This device is used as the common-emitter portion of a current-source-loaded cascode connection operating at a quiescent current of 10 μA. The second cascode transistor can either be a bipolar device with parameters as given above or a FET with $y_{fs} = 10^{-4}$ mho and $y_{os} = 10^{-6}$ mho. (See Fig. 8.19*b* for an incremental FET model.) Compare the voltage gain that results with these two options.

P8.11

Consider the amplifier shown in Fig. 8.34. The biasing is such that when all devices are in their linear operating regions, the quiescent operating current is 10 μA. Find the voltage gain of this connection assuming all four bipolar transistors have identical parameter values as do both FET's.

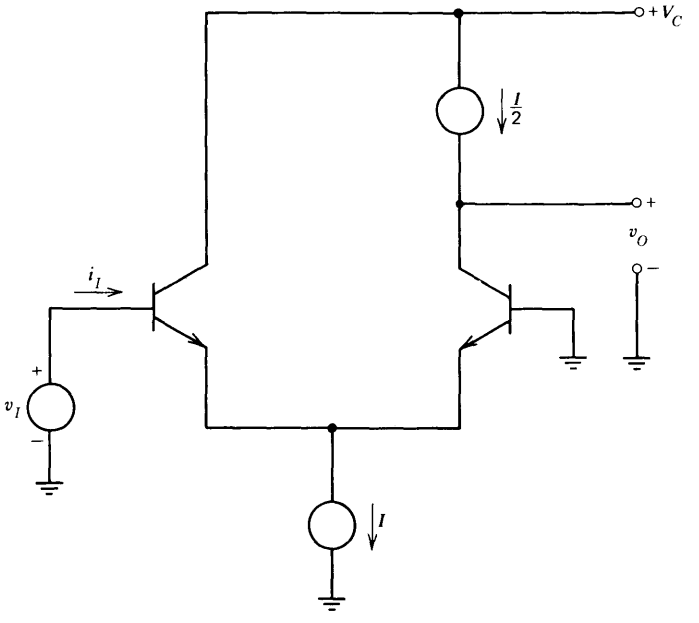

Figure 8.33 Current-source-loaded differential amplifier.

Use the values given in Problem P8.10. Estimate the break frequency of the dominant pole in the amplifier transfer function assuming that both FET's have drain-to-gate capacitances of 2 pF and that these capacitances dominate the frequency response.

P8.12

Determine the input resistance of the emitter-follower connection shown in Fig. 8.35 as a function of transistor parameters and quiescent operating levels. You may assume both transistors are identical.

P8.13

Thermal runaway is a potentially destructive process that can result when a transistor operates at fixed base-to-emitter and collector-to-emitter voltage because of the following sequence of events. The device heats up as a consequence of power dissipated in it. This heating leads to a higher collector current, a correspondingly higher power dissipation, and consequently a further increase in temperature. The objective of this problem is to determine the conditions under which unbounded thermal runaway results.

The transistor in question is biased with a fixed collector-to-emitter voltage of 10 volts, and fixed base-to-emitter voltage that yields a quiescent collector current I_C. You may assume the transistor has a large value for β,

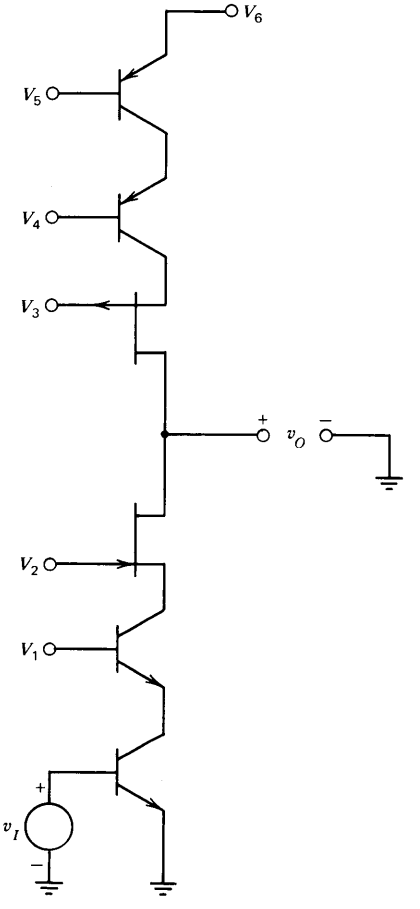

Figure 8.34 High-gain amplifier.

and that transistor base-to-emitter voltage, collector current, and temperature are related by Eqn. 7.1. The constant A in this equation is such that the transistor collector current is 10 mA at 0° C chip temperature with a base-to-emitter voltage of 650 mV.

The device is operating at an ambient temperature of 0° C. Measurements indicate that chip temperature is linearly related to power dissipation. The transfer function relating these two quantities is

$$\frac{T_j(s)}{P_d(s)} = 100\left(\frac{1}{10^{-3}s + 1} + \frac{1}{100s + 1}\right)$$

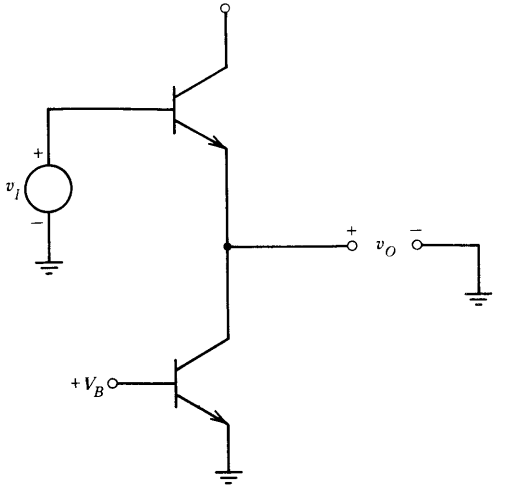

Figure 8.35 Emitter follower.

where T_j is the junction temperature in degrees Centigrade and P_d is the device power dissipated in watts.

Form a linearized block diagram that allows you to investigate the possibility of thermal runaway. Determine the quiescent value of I_C that results in transistor destruction. Now modify your block diagram to show how the inclusion of a transistor emitter resistor increases the safe region of operation of the connection.

P8.14

A certain operational amplifier can supply an output current of $\pm$ 5 mA over an output voltage range of ± 12 volts. Design a unity-voltage-gain stage that can be added to the output of the operational amplifier to increase the output capability of the combination to at least ± 100 mA over a ± 10-volt range. Available power-supply voltages are ± 15 volts. Assume that complementary transistors with a minimum β of 50 and a power dissipation capability of 2.5 watts are available. A reasonable selection of low power devices is also available. Your design should include current limiting to protect it for shorts from the output of the stage to ground.

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