CHAPTER VII

DIRECT-COUPLED AMPLIFIERS

7.1 INTRODUCTION

Operational amplifiers incorporate circuit configurations that may be relatively unfamiliar to the circuit designer with a background in other areas. An understanding of these special techniques is necessary for the most effective use of operational amplifiers.

One of the more challenging problems arises in the design of the input stage of an operational amplifier. One important consideration is that this stage provides gain to zero frequency. Thus the usual biasing techniques which incorporate capacitors that reduce low-frequency gain cannot be used. Circuits that provide useful gain at zero frequency are called *direct-coupled* or *direct-current* (d-c) *amplifiers*. The design of the direct-coupled input stage[1] of an operational amplifier is further complicated by the fact that it should have low input current.

Direct-coupled amplifiers are also useful other than as the input stage of an operational amplifier. Applications include processing certain signals of biological or geological origin that may contain significant components at a fraction of a hertz. While bandpass amplifiers can theoretically be used for such signals, the various capacitors required may become prohibitively large or expensive. Furthermore, the recovery time associated with large capacitors following overload or turn on is intolerable in some applications. In other cases, signals of interest contain frequencies of cycles per week, and response to zero frequency is mandatory in these situations. Alternatively, the designer may be interested in realizing a high-frequency amplifier, where minimization of capacitance to ground at certain critical nodes is of primary concern. If a large coupling capacitor is used, its stray capacitance to ground can deteriorate high-frequency performance.

The design of d-c amplifiers poses new problems because of the *drift* associated with such amplifiers. Drift is a phenomena whereby the output

[1] It is obviously necessary that all stages of an operational amplifier be direct coupled if the complete circuit is to provide useful gain at zero frequency. Emphasis here is given to the input stage because it represents the most challenging design problem.

of an amplifier changes not because of a change in the input voltage applied to the amplifier but rather in response to changes in circuit elements. In direct-coupled circuits, it is not possible to distinguish between an output that is a result of an applied input signal and one that occurs in response to drift. For this reason, drift limits the minimum input signal that can be detected.

A new circuit technique is required for the design of an amplifier that provides sufficiently low drift to be useful in d-c applications. In this chapter we shall concentrate on one circuit, the differential amplifier, which is used almost exclusively for d-c amplification. This circuit is particularly valuable when realized with bipolar transistors, since their highly predictable characteristics are readily exploited to yield low-drift performance.[2]

The discussion in this chapter focuses on the techniques used to reduce the drift and input current of a d-c amplifier, and thus the techniques described are useful in a range of applications. Toward the end of expanding the applicability of the techniques described in this chapter, certain aspects are covered in greater detail than is necessary for a basic understanding of operational amplifiers. Thus, as is the case with the material on feedback systems, operational amplifiers are used as a vehicle for illustrating technology valuable in a variety of electronic circuit and system design problems. The specific ways that these design techniques are incorporated into operational amplifiers are reserved for discussion in subsequent sections.

7.2 DRIFT REFERRED TO THE INPUT

The most useful measure of the drift of an amplifier is a quantity called *drift referred to the input*, and unless specifically stated otherwise, this quantity is the one implied when the term drift is used. Drift referred to the input is defined with reference to Fig. 7.1. This figure shows an amplifier with an assumed desired output voltage of zero for zero input voltage. The amplifier is initially *balanced* by making $v_I = 0$, and adjusting some amplifier parameter (shown diagrammatically in Fig. 7.1 as a variable resistor) until $v_O = 0$. An external quantity, such as temperature, supply voltage, or time, is then changed and, if the amplifier is sensitive to this quantity, its output voltage changes. An input voltage is then applied to the amplifier, and v_I is adjusted until v_O again equals zero. The drift referred to the

[2] A humorous comment on the difficulty of achieving acceptable d-c amplifier performance before modern bipolar transistors were developed is provided in L. B. Argumbau and R. B. Adler, *Vacuum-Tube Circuits and Transistors*, Wiley, New York, 1956. Chapter III, section 15 of this book is titled "Direct-Voltage Amplifiers—Why to Avoid Building Them."

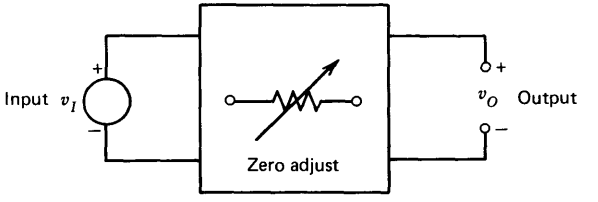


Figure 7.1 System used to define drift referred to the input.

input of the amplifier is equal to the value of v_I necessary to zero the output. The resultant magnitude is often normalized and specified, for example, as volts per degree Centigrade, volts per volt (of supply voltage), or volts per week. The minimum-detectable-signal aspect of this definition is self-evident.

In many situations we are concerned not only with the variability of the circuit as some external influencing factor is changed, but also with uncertainties that arise from the manufacturing process. In these cases, rather than initially balancing the circuit, the voltage that must be applied to its input to make its output zero may be specified as the *offset referred to the input*. The specifications related to drift and offset are at times combined by listing the maximum input offset that will result from manufacturing variations and over a range of operating conditions.

There is a tendency to use an alternative (incorrect) definition of drift, which involves dividing the drift measured at the output of the amplifier by the amplifier gain. The difficulty in this approach arises since the gain is frequently dependent on the drift-stimulating variable.

While alternative measurements of drift or offset may be equivalent in special cases, and are often used in the laboratory to simplify a measurement procedure, it is necessary to insure equivalence of other methods for each circuit. We shall normally use the original definitions for our calculations.

Figure 7.2 shows a very simple amplifier, which will be used to illustrate drift calculations and to determine how the base-to-emitter voltage of a bipolar transistor changes with temperature. It is assumed that the drift of the circuit with respect to temperature is required, and that the initial temperature is 300° K. It is further assumed that for the transistor used, $i_C = 1$ mA at $v_{BE} = 0.6$ V and $T = 300°$ K. With $v_I = 0$, these parameters show that it is necessary to adjust the potentiometer to its midposition to make $v_O = 0$. The temperature is then changed to 301° K, and it is observed the v_O is negative. (The amount is unimportant for our purposes.) In order to return v_O to zero (required by our definition of drift), it is necessary to return the transistor collector current to its original value. The change in

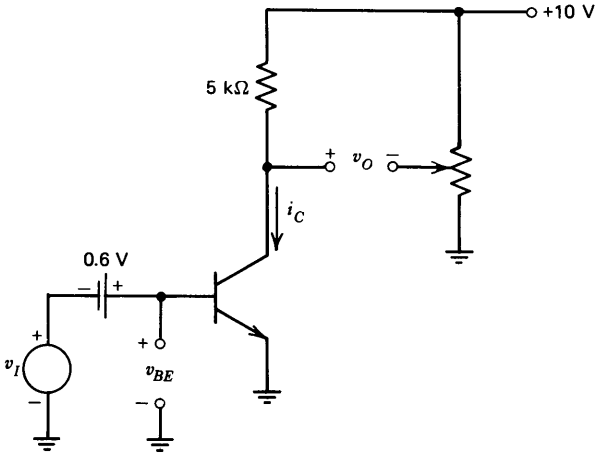


Figure 7.2 Circuit illustrating drift calculation.

v_{BE} required to restore collector current is identically equal to the required change in v_I and is therefore, by definition, the drift referred to the input of the amplifier. This discussion shows that drift for this circuit can be evaluated by determining how v_{BE} must vary with temperature to maintain constant collector current.

Drift for the circuit shown in Fig. 7.2 can be determined from the relationship between transistor terminal variables and temperature. If ohmic drops are negligible and the collector current is large compared to the saturation current I_S[3]

$$i_C = I_S e^{q v_{BE}/kT} = AT^3 e^{qV_{go}/kT} e^{qV_{BE}/kT} = AT^3 e^{q(v_{BE}-V_{go})/kT} \tag{7.1}$$

where A is a constant dependent on transistor type and geometry, q is the charge on an electron, k is Boltzmann's constant, T is the temperature, and V_{go} is the width of the energy gap extrapolated to absolute zero divided by the electron charge ($V_{go} = 1.205$ volts for silicon).[4] It is possible to verify the exponential dependence of collector current on base-to-emitter voltage experimentally over approximately nine decades of operating current for many modern transistors.

[3] P. E. Gray et al., *Physical Electronics and Models of Transistors*, Wiley, New York, 1964.

[4] There is disagreement among authors concerning the exponent of T in Eqn. 7.1, with somewhat lower values used in some developments. As we shall see, the quantity has relatively little effect on the final result. (The exponent appears only as a multiplying factor in the final term of Eqn. 7.5 and as a coefficient in Eqn. 7.8). Furthermore, two similar transistors should have closely matched values for this exponent, and the degree of match between a pair is the most important quantity in anticipated applications.

Solving Eqn. 7.1 for v_{BE} yields

$$v_{BE} = \frac{kT}{q} \ln \frac{i_C}{AT^3} + V_{go} \tag{7.2}$$

The partial derivative of v_{BE} with respect to temperature at constant i_C is the desired relationship, and

$$\left.\frac{\partial v_{BE}}{\partial T}\right|_{i_C = \text{const}} = \frac{k}{q} \ln \frac{i_C}{AT^3} - \frac{3k}{q} \tag{7.3}$$

However, from Eqn. 7.2

$$\frac{k}{q} \ln \frac{i_C}{AT^3} = \frac{v_{BE} - V_{go}}{T} \tag{7.4}$$

Substituting Eqn. 7.4 into Eqn. 7.3 yields

$$\left.\frac{\partial v_{BE}}{\partial T}\right|_{i_C = \text{const}} = \frac{v_{BE} - V_{go}}{T} - \frac{3k}{q} \tag{7.5}$$

The quantity $v_{BE} - V_{go}/T$ is -2 mV/°C at $T = 300°$ K for the typical v_{BE} value of 0.6 volt. The term $3k/q = 0.26$ mV/°C; therefore to a good degree of approximation

$$\left.\frac{\partial v_{BE}}{\partial T}\right|_{i_C = \text{const}} \simeq \frac{v_{BE} - V_{go}}{T} \tag{7.6}$$

The approximation of Eqn. 7.6 links the two rule-of-thumb values of 0.6 V and -2 mV/°C for the magnitude and temperature dependence, respectively, of the forward voltage of a silicon junction.

It is valuable to note two relationships that are exploited in the design of transistor d-c amplifiers. First, with no approximations beyond those implied by Eqn. 7.1, it is possible to determine the required transistor base-to-emitter voltage variation for constant collector current knowing only the voltage, the temperature, and the material used to fabricate the transistor. Furthermore, if two silicon (or two germanium) transistors have identical base-to-emitter voltages at one temperature and at certain (not necessarily identical) operating currents, the temperature coefficients of the base-to-emitter voltages must be equal. Second, the base-to-emitter temperature coefficient at any one operating current is very nearly independent of temperature as shown by the following development. The variation of temperature coefficient with temperature is found by differentiating Eqn. 7.5 with respect to temperature, yielding

$$\frac{\partial}{\partial T}\left[\frac{\partial v_{BE}}{\partial T}\right]_{i_C = \text{const}} = \frac{-(v_{BE} - V_{go}) + T(\partial v_{BE}/\partial T)}{T^2} \tag{7.7}$$

Substituting from Eqn. 7.5 for the $\partial v_{BE}/\partial T$ term in Eqn. 7.7, we obtain

$$\frac{\partial}{\partial T}\left(\frac{\partial v_{BE}}{\partial T}\right) = -3k/qT \tag{7.8}$$

Evaluating Eqn. 7.8 at 300° K shows that the magnitude of the change in base-to-emitter voltage temperature coefficient with temperature is less than 1 μV/°C/°C.[5]

It is now possible to determine the drift referred to the input of our original amplifier. In order to return v_O in Fig. 7.2 to zero at the elevated temperature, it is necessary to decrease i_C to its original value of 1 mA, and this decrease requires a -2.26 mV change in v_I (Eqn. 7.5). The drift referred to the input of our amplifier is by definition -2.26 mV/°C, and Eqn. 7.8 insures that this drift is essentially constant over a wide range of temperatures.

7.3 THE DIFFERENTIAL AMPLIFIER

The highly predictable temperature coefficient of the base-to-emitter voltage of a bipolar transistor offers the possibility that some type of compensation can be used to produce low-drift amplifiers. It is evident that the use of one transistor junction to compensate for voltage variations of a second similar junction should provide excellent results since both devices vary in a similar way. This section describes a connection that exploits the characteristics of a pair of bipolar transistors to provide low drift combined with several other useful features.

7.3.1 Topology

Consider the connection shown in Fig. 7.3. Here transistor Q_2 is connected as a common-base amplifier, while transistor Q_1 is connected as an emitter follower. Assume that initially $v_{I1} = 0$, that the two transistors are at the same temperature and that they are matched in the sense that they have identical saturation currents. In this case the voltages at the emitters of the two transistors will be equal, or $v_{O1} = v_{I2}$. The connection shown as a dotted line can then be completed with no change in any voltage level. If the magnitude of the voltage V_2 is much larger than anticipated variations in base-to-emitter voltage, the current through parallel resistor combination is virtually temperature independent. The matched transistor characteristics insure that this constant current divides equally between the

[5] An interesting alternative development of this relationship is given in "An Exact Expression for the Thermal Variation of the Emitter Base Voltage of Bi-Polar Transistors," R. J. Widlar, National Semiconductor Corp., Technical Paper TP-1, March, 1967.

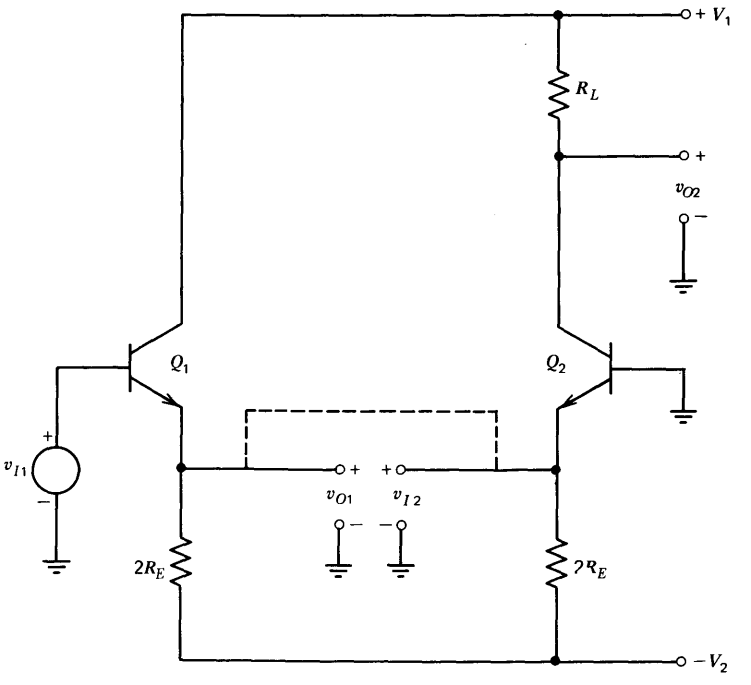


Figure 7.3 Circuit illustrating development of the differential amplifier.

two transistors. If we also assume that the common-base current gain of transistor Q_2 is one, changes in temperature result in negligible changes in the collector current of this device. Thus the drift referred to the input of this connection can be close to zero. In addition to providing temperature compensation, the current gain and input resistance of transistor Q_1 increases the input-resistance of the circuit by a factor of 2β above that seen at the emitter of Q_2.

The circuit that results when the dotted connection in Fig. 7.3 is completed is shown in Fig. 7.4. The inherent symmetry of the differential amplifier has been emphasized by including a collector-load resistor for Q_1 and permitting input signals to be applied to either base. A second output signal is indicated between the collectors of the two transistors in Fig. 7.4, so that both *differential* (between collector) or *single-ended* (either collector to ground) outputs are available.

7.3.2 Gain

The output of the circuit of Fig. 7.4 for any particular input voltage can be calculated by the usual methods. However, an alternative and useful

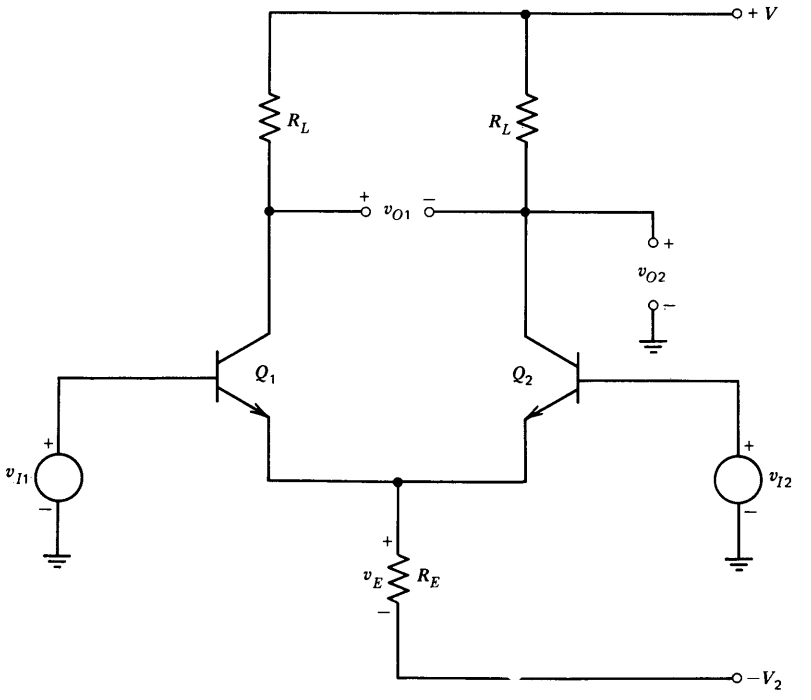


Figure 7.4 The differential amplifier.

analytic technique is available[6] that simplifies the calculations and gives greater insight into the operation of the circuit. The gain of the circuit is calculated for two particular types of inputs, a *differential* input with $v_{I1} = -v_{I2}$, and a *common-mode* input with $v_{I1} = v_{I2}$.

Figure 7.5 shows a schematic where the transistors have been replaced by appropriate, identical circuit models. Consider initially a pure differential input, of sufficiently small size so that the linear-region model remains valid. It is easily shown that in this case the voltage v_e does not change and that the common emitter connection may therefore be considered an incrementally grounded point. The incremental model for either half circuit reduces to that shown in Fig. 7.6. The incremental gain to the single-ended output, v_{o2}, is simply that of a common-emitter amplifier:

$$\left.\frac{v_{o2}}{v_{i2}}\right|_{v_{i1} = -v_{i2}} = \frac{-g_m R_L r_\pi}{r_x + r_\pi} \tag{7.9}$$

[6] An essentially identical analysis is given for vacuum-tube differential amplifiers in T. S. Gray, *Applied Electronics*, 2nd Ed., Wiley, New York, 1954, pages 504–509.

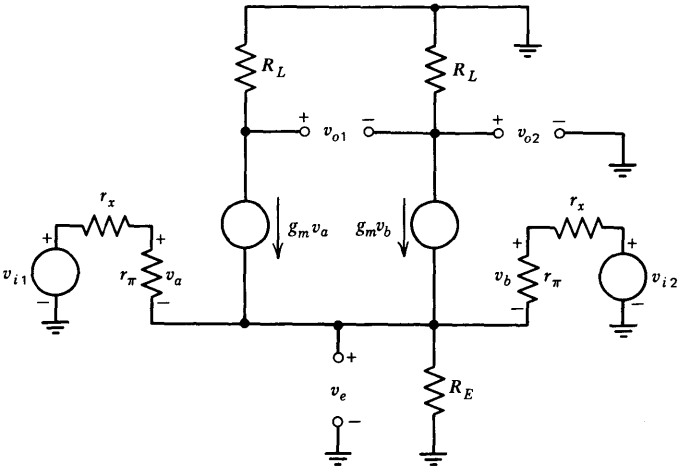


Figure 7.5 Incremental model for a differential amplifier.

The differential output component of v_{o1} for the left-hand half circuit is identical in magnitude but opposite in sign to that of the right-hand half circuit; therefore, $v_{o2} = -\frac{1}{2} v_{o1}$. The incremental gain to a differential output is then

$$\left.\frac{v_{o1}}{v_{i2}}\right|_{v_{i1} = -v_{i2}} = \frac{2g_m R_L r_\pi}{r_x + r_\pi} \tag{7.10}$$

It is conventional to consider gains calculated for a differential input signal applied between two bases of the amplifier, rather than by assuming a signal applied to one base and its negative applied to the other. If the signal between the bases is $e_d = 2\, v_{i1} = -2\, v_{i2}$ the gains become

$$\frac{v_{o2}}{e_d} = \frac{g_m R_L r_\pi}{2(r_x + r_\pi)} \tag{7.11}$$

and

$$\frac{v_{o1}}{e_d} = \frac{-g_m R_L r_\pi}{r_x + r_\pi} \tag{7.12}$$

For a pure common-mode input the voltage ($v_{i1} = v_{i2}$), symmetry insures that voltage v_{o1} (Fig. 7.5) remains zero and that $v_a = v_b$. Therefore, it is possible to "fold" the circuit about its vertical midline and parallel corresponding components. The resulting incremental model is shown in

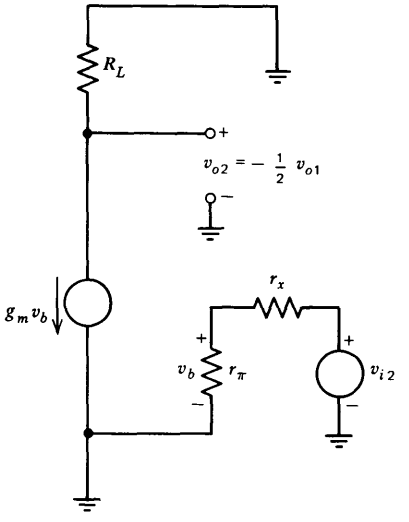


Figure 7.6 Right-hand half circuit for a differential input.

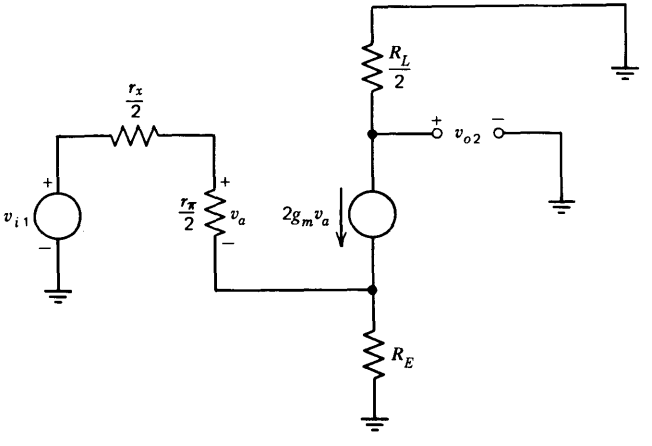


Figure 7.7 Circuit model for common-mode inputs.

Fig. 7.7. The gain to a single-ended output is identical to that of a common-emitter amplifier with emitter degeneration:

$$\left.\frac{v_{o2}}{v_{i1}}\right|_{v_{i1} = v_{i2}} = \frac{-g_m R_L r_\pi}{2[r_\pi/2 + r_x/2 + (\beta + 1)R_E]} \tag{7.13}$$

The common-mode input to differential-output gain is zero since v_{o1} does not change in response to a common-mode input signal.

While the gain of the differential amplifier has been calculated only for two specific types of input signals, any input can be decomposed into a sum of differential and common-mode signals. The output to each individual component can be calculated and, because of linearity, the output is the sum of the responses to the two individual inputs. For example, assume inputs e_a and e_b are applied to the left- and right-hand inputs of the circuit, respectively. The decomposition yields a common-mode component $e_{cm} = (e_a + e_b)/2$, and a differential component (applied between inputs) $e_d = e_a - e_b$. The physical implication is clear. It is assumed that any combination of input voltage levels is actually the sum of two signals: a common-mode signal (the two bases are incremented by equal amounts) equal to the average level, and a differential signal (the two bases are incremented by equal-magnitude, opposite-polarity signals) equal to the voltage applied between inputs.

7.3.3 Common-Mode Rejection Ratio

The evolution of the name differential amplifier is evident when we realize that circuit element values are typically such that the gain to a differential signal is significantly higher than that to a common-mode signal. The ratio of differential gain to common-mode gain is called the *common-mode rejection ratio* (CMRR), and many applications require high CMRR. For example, an electrocardiogram is a recording of the signal that results as the heart contracts, and is useful for the diagnosis of certain types of heart disease. The desired signal, detected by means of two electrodes attached to the body, has an amplitude of approximately 1 mV. In addition to the desired signal, a noise component at the power-line frequency with an amplitude of as much as 0.1 volt may be present as a common-mode signal on both electrodes. An amplifier with sufficiently high CMRR can be used to separate the desired signal from the interfering noise.

The analysis of Section 7.3.2 indicates that the common-mode rejection ratio of a differential amplifier with the output taken between collectors should be infinite. (As we shall see, this result is a consequence of the idealized model used.) The CMRR for a single-ended-output differential amplifier is obtained by dividing Eqn. 7.11 by Eqn. 7.13 yielding the magnitude

$$\text{CMRR} = \frac{r_\pi/2 + r_x/2 + (\beta + 1)R_E}{r_\pi + r_x} \tag{7.14}$$

Typically, $(\beta + 1)R_E \gg r_\pi \gg r_x$, so that

$$\text{CMRR} \simeq \frac{(\beta + 1)R_E}{r_\pi} \simeq g_m R_E \tag{7.15}$$

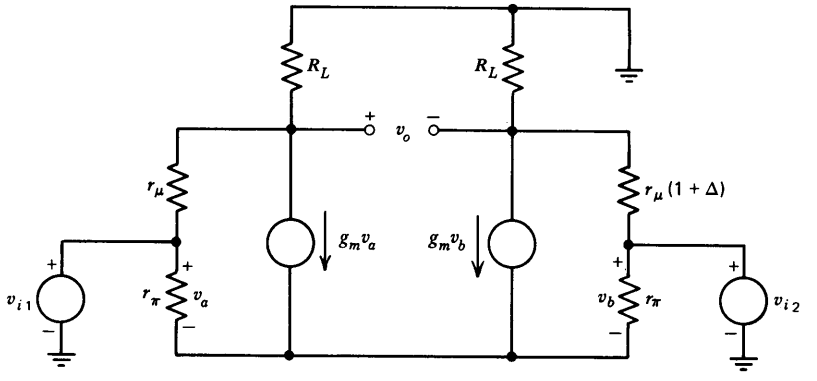


Figure 7.8 Circuit illustrating effect of unequal r_μ's.

Since the quiescent current through R_E (Fig. 7.4) is equal to twice the emitter current of either transistor, the CMRR can be related to V_E, the quiescent voltage across R_E, by

$$\text{CMRR} = \frac{q}{kT}\frac{V_E}{2R_E}R_E \simeq 20V_E \tag{7.16}$$

Equation 7.16 shows that one way to achieve high common-mode rejection ratios for single-ended-output differential amplifiers is to use a large bias voltage. An attractive alternative (which allows more moderate supply voltage) is the use of a current source (realized with a transistor with emitter degeneration) in place of R_E. This approach has the further advantage that the quiescent current level is independent of the common-mode input signal, and for these reasons most high-performance d-c amplifiers include an emitter-circuit current source.

If the simplified transistor model used up to now were strictly valid, the CMRR for an amplifier with an emitter-circuit current source would be infinite regardless of whether a single-ended or a differential output is used, since the incremental resistance of the current source (which replaces R_E in Eqn. 7.15) is infinite. Analysis based on a more complete model shows that it is not possible to achieve infinite CMRR with a single-ended output, but that CMRR can be made arbitrarily high for a differential-output amplifier by matching all transistor parameters sufficiently closely. It is useful to illustrate the degradation that results from imperfect matching by example. Figure 7.8 shows a linear-region equivalent circuit for a differential amplifier. A collector-to-base resistance has been included in the transistor

model.[7] The physical reason for the presence of this element in the model is described in Section 8.3.1. The magnitude of this resistance is r_μ for one transistor, while that of the second device differs by a fraction Δ. All other circuit parameters are identically matched. It is assumed that r_x is negligibly small compared to r_π.[8] It is further assumed that the circuit has been constructed with an ideal emitter-circuit current source. Since $r_\mu \gg R_L$, the gain for a differential input is

$$\left.\frac{v_o}{(v_{i2} - v_{i1})}\right|_{v_{i1} = -v_{i2}} = g_m R_L \tag{7.17}$$

The gain for a common-mode input is

$$\left.\frac{v_o}{v_{i1}}\right|_{v_{i1} = v_{i2}} = \frac{\Delta R_\mu R_L}{(R_L + r_\mu)[(1 + \Delta)r_\mu + R_L]} \tag{7.18}$$

Again invoking the inequality $r_\mu \gg R_L$ leads to

$$\left.\frac{v_o}{v_{i1}}\right|_{v_{i1} = v_{i2}} \simeq \frac{\Delta R_L}{(1 + \Delta)r_\mu} \tag{7.19}$$

The resultant CMRR is obtained by dividing Eqn. 7.17 by Eqn. 7.19, yielding

$$\text{CMRR} = \frac{g_m(1 + \Delta)r_\mu}{\Delta} \tag{7.20}$$

A similar approach can be used to calculate common-mode errors that arise from other sources such as unequal transistor collector-to-emitter resistance or unequal values of r_x. It can be shown that since each of these effects is small, there is little interaction among them, and it is valid to compute each error separately.

As a matter of practical interest, it is possible to obtain well enough matched transistors to obtain low-frequency values for CMRR on the order of 10^4 to 10^6 with a simple differential-amplifier connection.

[7] We shall also see that an additional resistor between collector and emitter is necessary to complete the model. This second resistor is omitted from the present discussion since the simplified model illustrates the point adequately.

[8] This assumption is frequently valid in the analysis of d-c amplifiers because the transistors are usually operated at low currents to decrease input current and to minimize offsets from differential self-heating. The resistance r_π grows approximately inversely with collector current, while the value of r_x is bounded, with a usual maximum value of 100 to 200 Ω. A typical value for r_π for transistors such as the 2N5963 is 2.5 MΩ at an operating current of 10 μA.

7.3.4 Drift Attributable to Bipolar Transistors

The reason for the almost exclusive use of the differential amplifier for d-c amplifier circuits is because of the inherent drift cancellation afforded by symmetrical components. The purpose of this section is to indicate how the circuit should be balanced for minimum drift.

If a differential amplifier such as that shown in Fig. 7.4 is constructed with symmetrical components, the differential output voltage v_{O1} is zero for $v_{I1} = v_{I2}$. While resistors are available with virtually perfectly matched characteristics, selection of well-matched transistors is a significant problem.

It has been assumed up to this point that the transistors used in a differential amplifier are matched in the sense that they have equal saturation currents. One measure of the degree of match is to specify the ratio of the saturation currents for a pair of transistors. This ratio is exactly the same as the ratio of the collector currents of the two transistors when operated at equal base-to-emitter voltages, since at a base-to-emitter voltage V_{BE} (assuming operation at currents large compared to I_S), the collector current of one transistor is

$$I_{C1} = I_{S1}e^{qV_{BE}/kT} \tag{7.21}$$

while that of the second transistor is

$$I_{C2} = I_{S2}e^{qV_{BE}/kT} \tag{7.22}$$

Alternatively, the degree of match can be indicated by specifying the difference ΔV between the base-to-emitter voltages of the two transistors when both are operated at some collector current I_C. This specification implies that at some base-to-emitter voltage V_{BE}

$$I_{C1} = I_{S1}e^{qV_{BE}/kT} = I_C = I_{C2} = I_{S2}e^{q(V_{BE}+\Delta V)/kT} \tag{7.23}$$

This measure of match is easily related to the degree of match between saturation currents, since Eqn. 7.23 shows that

$$\frac{I_{S1}}{I_{S2}} = e^{q\Delta V/kT} \tag{7.24}$$

Equation 7.24 also shows that the base-to-emitter voltage mismatch, ΔV, is independent of the operating current level selected for the test.

If the circuit of Fig. 7.4 is used as a d-c amplifier, the quantity ΔV for the transistor pair is exactly the offset referred to the input of the amplifier, since this differential voltage must be applied to the input to equalize collector currents and thus make v_{O1} zero. For this reason, semiconductor manufacturers normally specify the degree of match between two transistors

in terms of their base-to-emitter voltage differential at equal currents rather than as the ratio of saturation currents.

Several options are available to the designer to obtain well-matched pairs for use in differential amplifiers. Matched transistors are available from many manufacturers at a cost of from 2 to 10 times that of the two individual devices. These transistors are frequently mounted in a single can so that the differential temperature of the two chips is minimized. The best specified match available in a particular series of devices is typically a 3-mV base-to-emitter voltage differential when the devices operate at equal collector currents.

An alternative involves user matching of the transistors. This possibility is attractive for several reasons. There are economic advantages, particularly if large numbers of matched pairs are required, since relatively modest equipment suffices and since the effort required is not prohibitive. Better matches for a greater number of parameters are possible than with purchased matched pairs. However, lack of money, patience, and environmental control (remember the typical temperature coefficient of -2 mV/°C) generally limits achievable base-to-emitter voltage matches to the order of 0.5 mV. It is also necessary to provide some sort of thermal coupling to keep the matched devices at equal temperatures during operation.

A third possibility is the use of a monolithic integrated-circuit differential pair. Through proper control of processing, all transistor parameters are simultaneously matched, and differential base-to-emitter voltages on the order of 1 mV are possible with present technology. Excellent thermal equality is obtained because of the proximity of the two devices. This approach is used as an integral part of all monolithic operational amplifiers. There are also a number of single and multiple monolithic matched pairs available for use in discrete designs. Several more sophisticated monolithic designs are available[9] that include temperature sensing and heating elements on the chip to keep its temperature relatively constant. The effects of ambient temperature variations are largely eliminated by this technique.

Regardless of the matching procedure used, some type of trimming is required to reduce the offset of the amplifier to zero at one temperature. One popular technique is to include a potentiometer in the emitter circuit as shown in Fig. 7.9. The two bases are shorted together and the pot is adjusted until the two collector currents are equal so that $v_O = 0$. This adjustment is possible for $R > 2\Delta V/I$, where ΔV is the base-to-emitter voltage differential of the pair at equal collector currents. (The use of too

[9] Examples include the Fairchild Semiconductor μA726 and μA727.

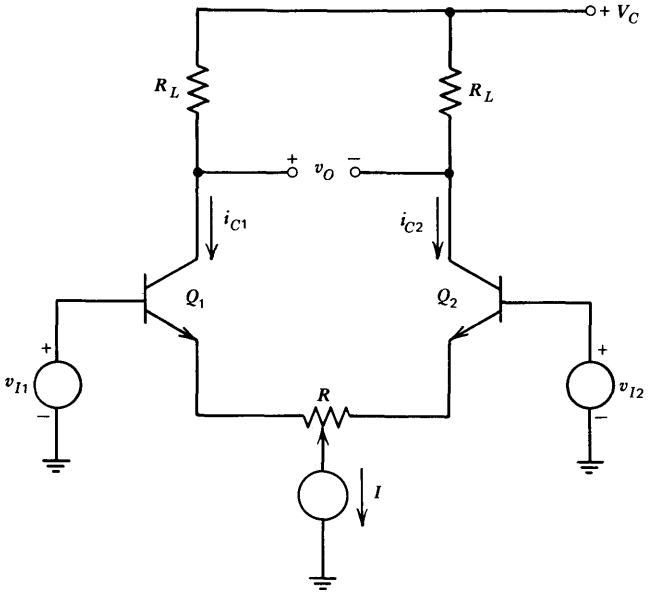


Figure 7.9 Balancing with emitter-circuit potentiometer.

large a potentiometer is undesirable since it lowers the transconductance[10] of the pair, and we shall see that this quantity becomes important when the effect of other circuit components on drift is considered.) While this balance method is frequently used, it is fundamentally in error if minimization of drift with temperature is the design objective. The approach equalizes collector currents and thus insures that one transistor operates at a quiescent base-to-emitter voltage of v_{BE1}, while the other operates at a voltage of $v_{BE1} + \Delta V$. The required difference in base-to-emitter voltages is obtained by adjusting the pot so that the voltages across its two segments differ by ΔV. Since the voltages across the pot segments are the same whenever the input voltage is adjusted to make v_O zero (assuming the common-base current gain of the transistors is one, the current through each pot segmen must be $I/2$ when $v_O = 0$), the drift referred to the input with respect to

[10] The transconductance of a differential pair is defined as the ratio of the incremental change in either collector current to the incremental differential input voltage. Assuming that both transistors have large values for β and negligible base resistance, the transconductance for the configuration shown in Fig. 7.9 is

$$\left|\frac{i_{c1}}{v_{i1} - v_{i2}}\right| = \left|\frac{i_{c2}}{v_{i1} - v_{i2}}\right| \simeq \frac{1}{1/g_{m1} + 1/g_{m2} + R}$$

temperature for this design is identically equal to the differential change in the transistor base-to-emitter voltages with temperature. From Eqn. 7.5,

$$\frac{\partial}{\partial T}(v_{BE1} - v_{BE2})\bigg|_{i_{C1} = i_{C2} = \text{const}} = \left(\frac{v_{BE1} - V_{go}}{T} - \frac{3k}{q}\right) - \left(\frac{v_{BE2} - V_{go}}{T} - \frac{3k}{q}\right) = \frac{v_{BE1} - v_{BE2}}{T} \tag{7.25}$$

Since the difference $v_{BE1} - v_{BE2}$ is ΔV,

$$\frac{\partial}{\partial T}(v_{BE1} - v_{BE2}) = \frac{\Delta V}{T} \tag{7.26}$$

For example, a 3-mV mismatch at room temperature leads to a drift of 10 μV/°C.

An alternative is to operate the transistors with equal base-to-emitter voltages. This condition requires that the quiescent collector-current ratio be equal to the ratio of the transistor saturation currents, or

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} = e^{q\Delta V/kT} \tag{7.27}$$

where, as defined above, ΔV is the difference between the base-to-emitter voltages of the two devices *when they are operated at equal collector currents.* In this case, a 3-mV value for ΔV requires a 12% difference in collector currents to equalize base-to-emitter voltages. A possible circuit configuration is shown in Fig. 7.10. The two bases are shorted together, which forces equal base-to-emitter voltages and zero differential input voltage. The potentiometer is then adjusted to make $v_O = 0$. The results of earlier analysis indicate that the temperature drift attributable to the transistors should be zero following this adjustment. While very low values are attainable by this method, there are other detailed effects, neglected in our simplified analysis, which lead to nonzero drift. It is possible to adjust the relative base-to-emitter voltages to compensate for these effects.[11] In practice, even the simplified balancing technique can result in drifts of a fraction of a microvolt per degree Centigrade.

It is stressed that this balancing technique should not be considered a substitute for careful matching of the devices, but rather as a final trim following matching. If a large base-to-emitter voltage mismatch is compensated for by this method, there is a large differential power dissipation with associated differential heating, base currents will differ by a large amount,

[11] A. H. Hoffait and R. D. Thornton, "Limitations of Transistor DC Amplifiers," *Proceedings Institute of Electrical and Electronic Engineers*, February, 1964.

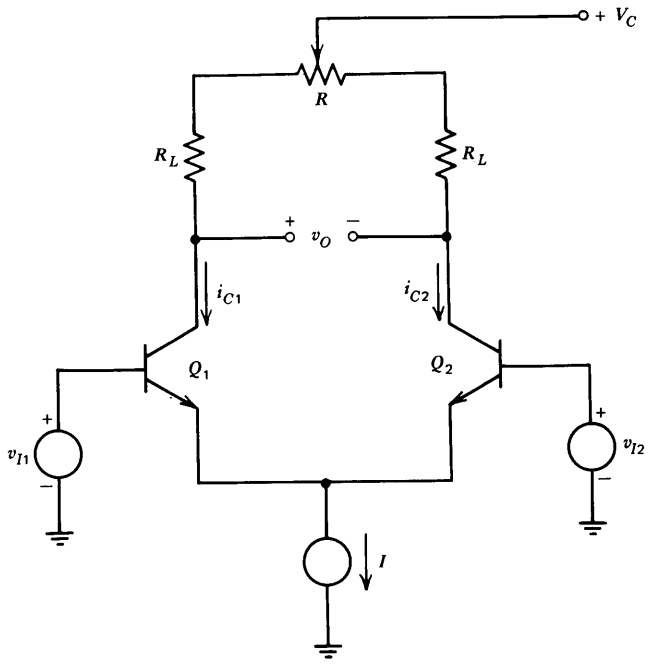


Figure 7.10 Method for balancing with equal base-to-emitter voltages.

and the transconductance of the pair will be significantly lower than if well-matched devices are used. For example, compensation for a 60-mV mismatch requires collector currents with a 10 to 1 ratio and lowers transconductance by a factor of five compared with a well-matched pair operated at the same total emitter current. Operation with severely unbalanced collector currents also mismatches all current-dependent transistor parameters.

7.3.5 Other Drift Considerations

It is interesting to note that the excellent compensation afforded by even the simplified balancing technique described above emphasizes the drift contribution of other components in circuit. Consider the circuit shown in Fig. 7.11. (For simplicity it is assumed that inputs are applied to only one side of the circuit.) Assume that the transistors are perfectly matched so that when the collector resistors are equal $v_O = 0$ for $v_I = 0$. A drift results if the relative collector-resistor values change as a result of differential changes with temperature or aging. The drift attributable to a collector-resistor fractional unbalance Δ can be calculated as follows. With $v_I = 0$, $i_{C1} = i_{C2} \simeq I/2$. As v_i is increased, $i_{C1} = I/2 + (g_m/2)v_i$ and $i_{C2} = I/2 - (g_m/2)v_i$, where g_m is the transconductance of either transistor. (It is as-

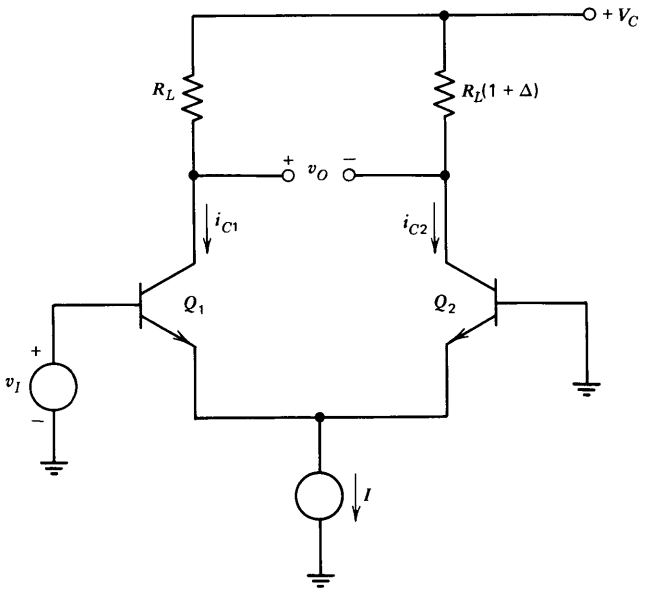


Figure 7.11 Circuit with unequal load resistors.

sumed that $r_\pi \gg r_x$ for the transistors.) In order to return v_O to zero, it is necessary to have

$$\left(\frac{I}{2} + \frac{g_m}{2} v_i\right)R_L = \left(\frac{I}{2} - \frac{g_m}{2} v_i\right)(1 + \Delta)R_L \tag{7.28}$$

or

$$g_m v_i = \frac{\Delta I}{2} \tag{7.29}$$

(A term containing the small cross product $g_m v_i \, \Delta R_L$ has been dropped.) Since each device is operating at a quiescent current level $I/2$, $g_m = qI/2kT \simeq 20I$ at room temperature. Thus the input voltage required to return the output voltage to zero (by definition the drift referred to the input) is $\Delta/40$. The significance of this sensitivity is appreciated when one considers that two ordinary equal-value carbon-composition resistors can have temperature coefficients that differ by as much as one part per thousand per degree Centigrade. Use of such resistors would result in an amplifier drift of 25 μV/°C! It is clear that the quality of the resistors used is an important factor when a 1 μV/°C amplifier is designed.

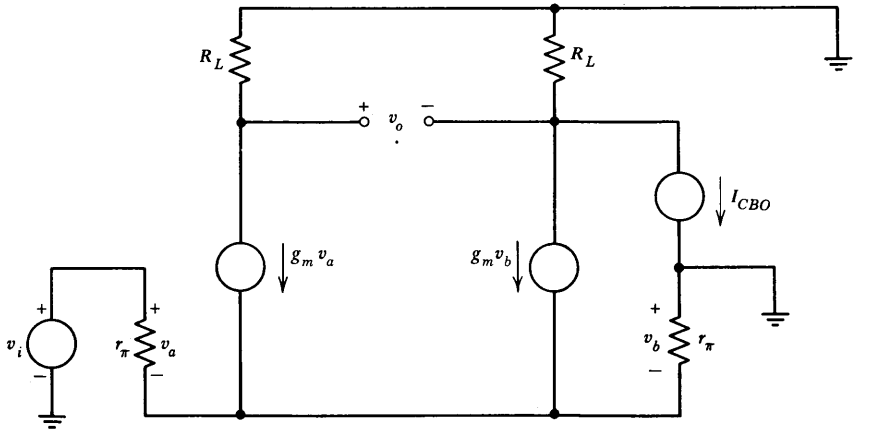


Figure 7.12 Equivalent circuit for finding drift as a function of I_{CBO}.

A similar conclusion is reached when the effects of collector-to-base leakage current I_{CBO}[12] are considered. An equivalent circuit that can be used to predict the drift from I_{CBO} is shown in Fig. 7.12. Since the magnitude of I_{CBO} is likely to be significantly different for two otherwise well-matched transistors, only one leakage current generator is shown in Fig. 7.12. Its value can be made the difference between the leakages if one component is not negligible. Proceeding as before, the value of v_i required to reduce the output to zero is given by solving

$$\frac{g_m v_i}{2} = \frac{-g_m v_i}{2} + I_{CBO} \tag{7.30}$$

for v_i, yielding

$$v_i = \frac{I_{CBO}}{g_m} \tag{7.31}$$

The transconductance of either input transistor g_m can be related to the bias level for the differential pair (each member operates at $I/2$) as $g_m = 20I$. Therefore, the offset expressed in volts is $I_{CBO}/20I$. Typical values are again evoked to illustrate the problem. The FT107A (an attractive choice for the input stage of a d-c amplifier since its specifications include a typical β of

[12] The assumptions often used to simplify device physics to the contrary, this quantity is not related to the saturation current in the transistor equation. The magnitude of I_S is dominated by effects within the body of the semiconductor, while the dominant component of I_{CBO}, at least at room temperature, results from surface effects. Temperature coefficients are significantly different. While I_S doubles every 6° C, I_{CBO} near room temperature typically doubles every 10° C.

1100 at 10 μA of collector current!) has a specified maximum leakage current that increases from essentially zero at 25° C to 1 μA at 125° C. The resultant average drift over the 100° C temperature range for the device operating at a collector current level of 10 μA ($I = 20$ μA) is therefore bounded by 25 μV/°C. Fortunately the typical value for I_{CBO} is 2% of the maximum specified value, but additional screening procedures are required to insure this lower level is met by any particular device.

It is worth emphasizing the importance of proper thermal design for low-drift d-c amplifiers. A temperature differential of 0.001° C results in an offset of 2 μV for a differential pair that is perfectly matched when the temperatures of the transistors are identical. Several factors influence the temperature differential of a pair. Good thermal contact between the members of the pair is mandatory. This required contact can be achieved by locating the two chips close together on a thermally conductive plate, or via monolithic integrated-circuit construction.

It is also necessary to minimize heating effects that disturb the pair. Self-heating as a consequence of the power dissipated in the pair is particularly important. Differential self-heating is reduced by operating the two members of the pair at matched, low collector currents and at low collector voltage. The location of other heat sources that can establish thermal gradients across the pair must also be considered. These sources are easily isolated in discrete-component designs, but impose severe constraints on component placement in integrated circuits.

Another aspect of the thermal problem involves the way in which the differential-amplifier transistors are connected to the input signal or to other circuit components. A thermocouple with an approximately 20 μV/°C coefficient is formed when kovar, an alloy frequently used for transistor leads, is connected to copper. Thus thermal gradients across the circuit, which result in different temperatures for series-connected thermocouple junctions in the signal path, can contribute significant offset voltage.

7.4 INPUT CURRENT

The discussion of input-circuit errors up to this point has focused on voltage drift referred to the input. Additional input offset signals arise from input current if the signal source resistance is high. In many d-c amplifiers constructed using bipolar transistors, offsets from input current dominate. One alternative is the use of junction-gate or metal-oxide-semiconductor (MOS) field-effect transistors that exhibit substantially lower input currents. Unfortunately, the voltage drift of junction-gate field-effect transistors is about one order of magnitude worse than that of bipolar devices. MOS de-

vices, with threshold voltages dependent on trapped surface charge, are even more unstable. The techniques used to stabilize the operation of these devices are significantly different than those used with bipolar transistors and are not discussed here.[13]

In contrast to the base-to-emitter voltage, which varies in a highly predictable fashion with temperature, the temperature dependence of base current is a complex function of transistor structure. Furthermore, matching most parameters of two transistors, including β at one temperature, does not insure equal current gain at some different temperature. As a matter of practical interest, the fractional change in current gain with temperature, $(1/\beta)(\partial\beta/\partial T)$, is typically 0.5 to 1% per degree Centigrade, with somewhat higher values measured at low collector currents and low temperatures.

While these unpredictable variations in β make input-current compensation schemes less precise than voltage-drift compensation, several useful methods are available for lowering input current.

7.4.1 Operation at Low Current

In spite of manufacturers' reluctance to admit it, there are many types of transistors that exhibit useful current gains at low collector currents. It is not unusual to find units with a value for β in excess of 10 at $I_C = 10^{-11}$ A, and devices with current gains of 100 at $I_C = 10^{-9}$ A are easily selected from several families. Clearly, operation at reduced collector current is one approach to low input current. A disadvantage of this technique is that collector-to-base leakage current may dominate input current, particularly at high temperatures, or may contribute to excessive voltage drift (see Section 7.3.5). However, I_{CBO} can be eliminated by operating a transistor at zero collector-to-base voltage, and there are several circuit techniques that keep this voltage low yet permit operation over a wide range of input voltages.

A more fundamental problem is the low f_T (current gain-bandwidth product) of devices operating at low collector currents. Below some current level the base-to-emitter capacitance C_π is dominated by a space-charge-layer capacitance, and this quantity is independent of current. Since collector-to-base capacitance C_μ is independent of operating current and g_m is directly proportional to current,

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{7.32}$$

is directly proportional to current at low operating currents. A typical value for f_T at a collector current of 1 nA is 1 kHz.

[13] L. Orchard and T. Hallen, "Fet Amplifier Design Precautions," *EDN*, August, 1968.

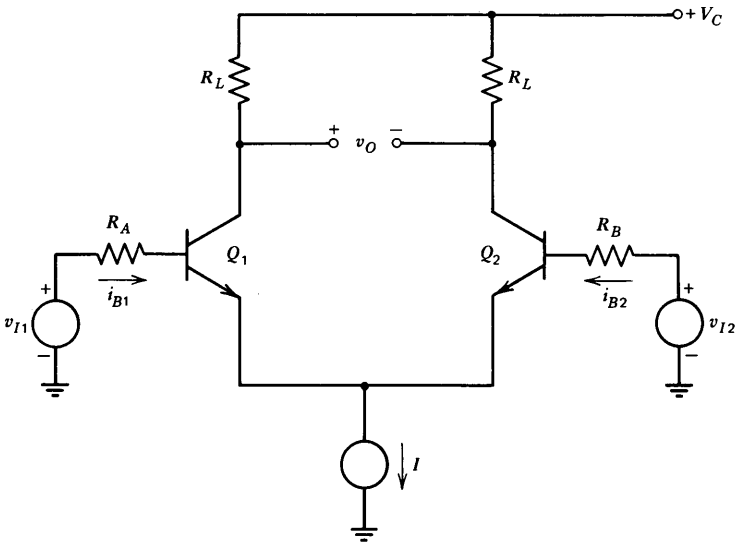


Figure 7.13 Method to eliminate effects of input current.

7.4.2 Cancellation Techniques

While the variation of input current with temperature is not as predictable as that of the base-to-emitter voltage, several compensation techniques take advantage of matching this quantity. Figure 7.13 shows one possibility. Here it is assumed that the source impedances associated with the two input signals are resistive and fixed. If

$$i_{B1}R_A = i_{B2}R_B \tag{7.33}$$

the drop across each source resistor is equal and the net effect is simply to apply a common-mode input signal to the amplifier.[14] Similarly, if

$$R_A \frac{\partial i_{B1}}{\partial T} = R_B \frac{\partial i_{B2}}{\partial T} \tag{7.34}$$

the effects of temperature-dependent input currents are eliminated. Both Eqns. 7.33 and 7.34 are satisfied if the resistors are selected to equalize voltage drops at one temperature and if the fractional change in β with temperature is equal for both devices. The technique of equalizing the re-

[14] It is assumed in this discussion that the input currents are independent of differential input voltage. This is not true for large signals, but in many applications the signals applied to a differential amplifier are sufficiently small to make base-current variations with signal level negligible. A technique to compensate for varying input current with signal levels is indicated in Section 7.4.3.

sistances connected to the two inputs (effectively assuming equal input currents) is frequently used in operational-amplifier connections.

In some applications, it is important to reduce the magnitude of one or both base currents of an amplifier, not simply insure that the two input currents to a differential amplifier are equal. Clearly one very simple approach is to provide the amplifier bias currents via resistors connected to an appropriate-polarity supply voltage. Unfortunately, the bias current supplied by this method is temperature independent, and thus the variation in amplifier input current with temperature is not decreased. Figure 7.14 shows one way to provide a degree of cancellation. If the β's of corresponding NPN and PNP transistors are equal, the current seen at either input is zero when the collector currents of the two NPN's are equal. The use of current sources in the emitters of the PNP's provides a compensating current that is independent of common-mode level.

Another technique is to use the temperature-dependent forward-voltage characteristics of a diode to generate a temperature-dependent compensating current, as shown in Fig. 7.15. The amplifier itself is shown diagrammatically in this figure, and only one input, close to ground potential, is indicated. Resistor R_1 establishes a bias current through the diode. It is assumed that this current is constant since it is selected to be much larger than i_A and that V_C is much greater than V_A and v_F. The temperature dependence of v_F, $\partial vF/\partial T$, is identical to that of a transistor (Eqn. 7.5) and is approxi-

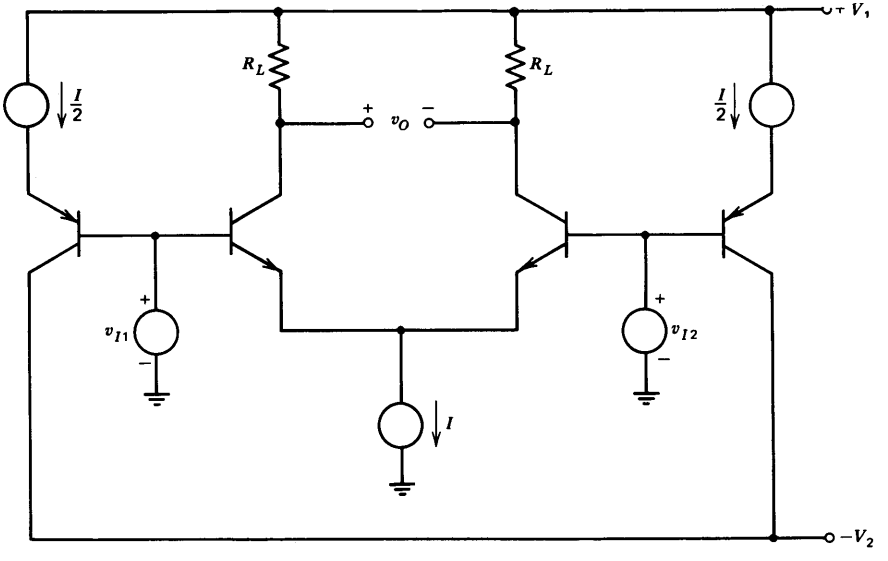


Figure 7.14 Input-current cancellation with transistors.

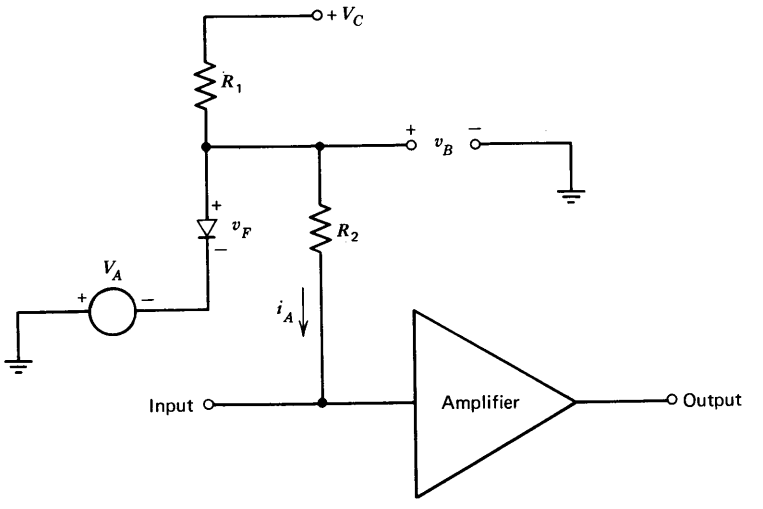


Figure 7.15 Use of a diode for input-current compensation.

mately constant with temperature.[15] The compensating current i_A is equal to v_B/R_2, and has a fractional change with temperature equal to

$$\frac{1}{i_A}\frac{\partial i_A}{\partial T} = \frac{1}{v_B}\frac{\partial v_B}{\partial T} = \frac{1}{(v_F + V_A)}\frac{\partial v_F}{\partial T} \tag{7.35}$$

The two degrees of freedom represented by the selection of V_A and R_2 can be used to cancel at one temperature both the input current and its first derivative with respect to temperature.

There are several variations on this basic topology that effectively bootstrap the reference voltage for the compensating diode from a node referenced to the common-mode input level such as the emitter connection of differential pair. The compensating current provided can be made relatively independent of common-mode level in this way, thus allowing the technique to be used with input voltages at arbitrary levels with respect to ground.

7.4.3 Compensation for Infinite Input Resistance

The compensation methods introduced up to this point have been intended to compensate for temperature variations of the input-transistor bias current. It has been assumed that the input signals are small enough

[15] Carrier recombination in a diode can multiply the $3k/q$ term in Eqn. 7.5 by a factor between one and two. This modification does not significantly alter the basic dependence.

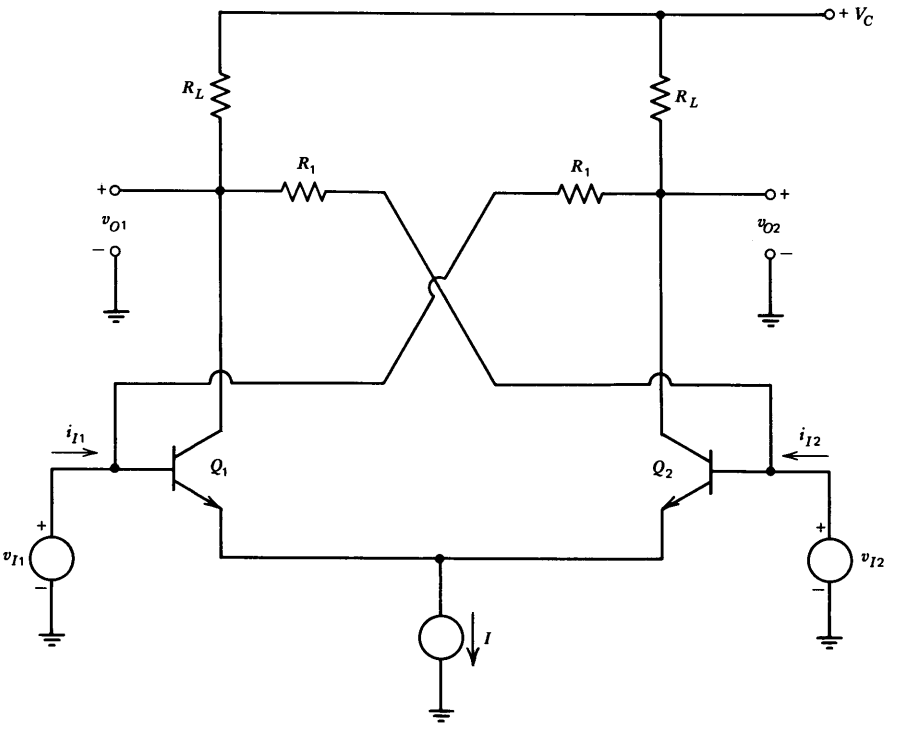


Figure 7.16 Circuit that can yield infinite differential input resistance.

so that the input-current component attributable to the input resistance of the amplifier is negligible. While this inequality is generally satisfied in applications (such as operational amplifiers) where the input circuit is followed by additional stages of voltage amplification, many differential-amplifier stages operate with appreciable differential signals applied to their input.

Figure 7.16 shows a connection that can be adjusted to provide infinite input resistance to differential signals. Consider a differential input signal, $v_{I1} = -v_{I2}$. A positive v_{I1} increases the current flowing into the base of Q_1 and causes a positive change in v_{O2}. By proper choice of parameters it is possible to supply the required base current through the right-hand R_1 so that the change in i_{I1} is zero[16]. The necessary value for R_1 is computed with the aid of the incremental model of Fig. 7.17. (The usual approximations

[16] This technique, which involves positive feedback, is not without its hazards. The topology of the circuit is essentially identical to that of a flip-flop, and if the circuit is overcompensated and driven from high impedance sources, bistable operation is possible.

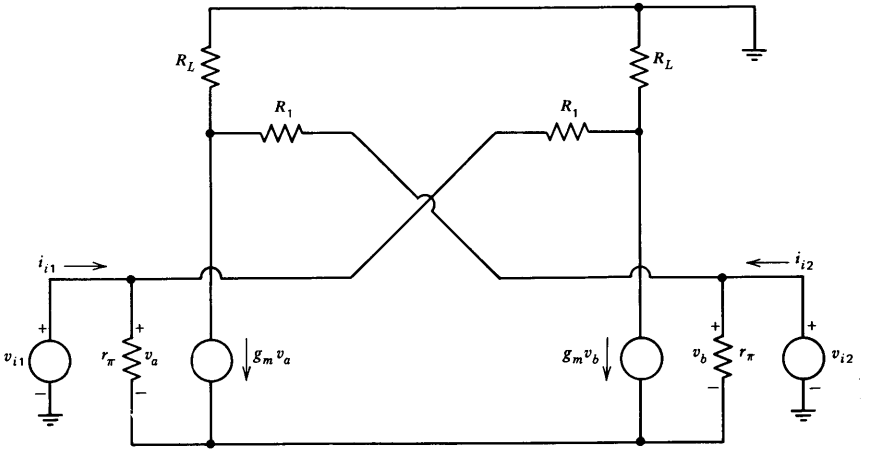


Figure 7.17 Increment model for circuit of Fig. 7.16.

have been included in developing the model.) Normally $R_1 \gg R_L$ so that the loading by R_1 can be neglected. With this assumption, the incremental input current i_{i1} that results for a pure differential input is

$$i_{i1} = v_{i1}\left[\frac{1}{r_\pi} - \left(\frac{g_m R_L - 1}{R_1}\right)\right] \tag{7.36}$$

If the voltage gain of the circuit is large so that $g_m R_L \gg 1$, the differential input resistance is infinite for

$$\frac{g_m r_\pi R_L}{R_1} = 1 \qquad \text{or } R_1 = \beta R_L \tag{7.37}$$

The common-mode input resistance is lowered by the compensating resistors, since Fig. 7.17 shows that

$$\left.\frac{v_{i1}}{i_{i1}}\right|_{v_{i1} = v_{i2}} = R_1 \tag{7.38}$$

High common-mode input resistance can be restored by including PNP transistors in this compensating circuit as shown in Fig. 7.18. In addition to supplying the compensating current from a high-resistance source, selection of the bias voltage gives an additional degree of freedom in controlling the quiescent level of the compensating current.

7.4.4 Use of a Darlington Input

One obvious way to lower input current is to use transistors with higher current gains. As mentioned earlier, transistors with current gains in ex-

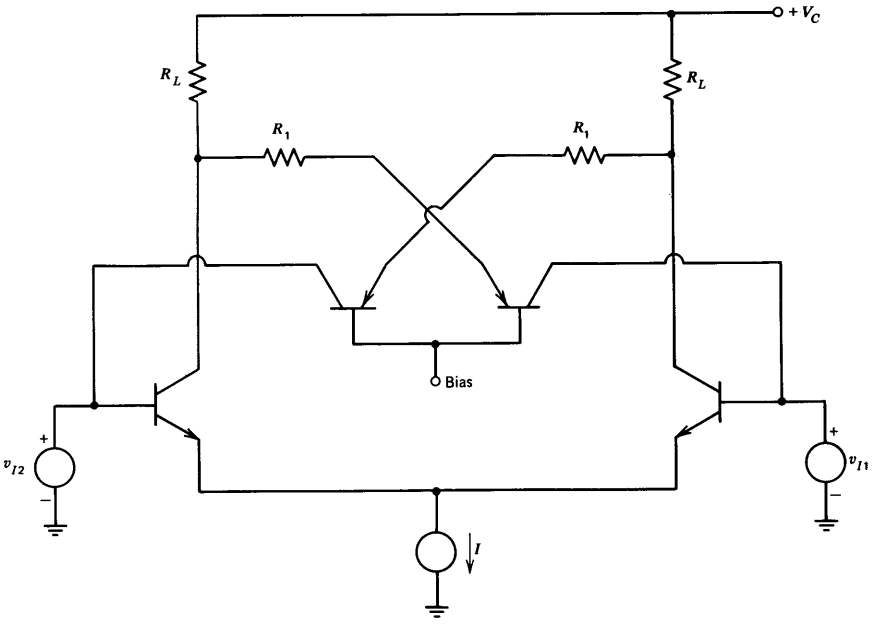


Figure 7.18 Use of common-base transistors to increase common-mode input resistance.

cess of 1000 are available, and this value should increase as processing techniques improve. It is also possible to use two transistors in the *Darlington connection* shown in Fig. 7.19. It is easy to show that at low frequencies this connection approximates a single transistor between terminals B, C, and E with current gain given by

$$\beta = \beta_2(\beta_1 + 1) + \beta_1 \simeq \beta_1\beta_2 \tag{7.39}$$

and a transconductance

$$g_m = \frac{q}{2kT} I_C \tag{7.40}$$

Current gains in excess of 10^5 are possible with available devices.

Figure 7.20 shows a differential amplifier with Darlington-connected input transistors. While a connection of this type yields low values for input current, the voltage drift for this configuration usually exceeds that of the conventional differential amplifier. The problem stems from differential changes in the base currents of transistors Q_1 and Q_2. (Remember that current gain varies in a relatively unpredictable way with temperature.) Since

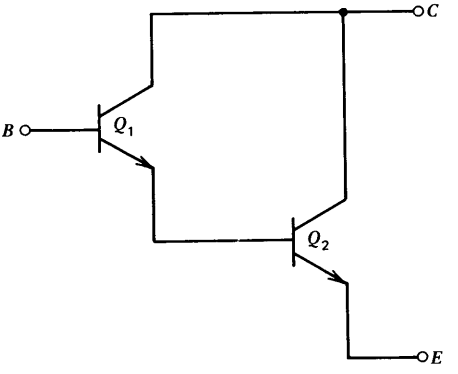


Figure 7.19 Darlington-connected transistors.

the resistance seen at the emitters of transistors Q_3 and Q_4 is relatively high, current changes produce significant changes in voltages v_A and v_B. A differential change in v_A and v_B results in drift equal in value to this change.

In order to compute drift referred to the input from this effect, it is necessary to determine how v_I must vary with i_A and i_B to keep $v_O = 0$.

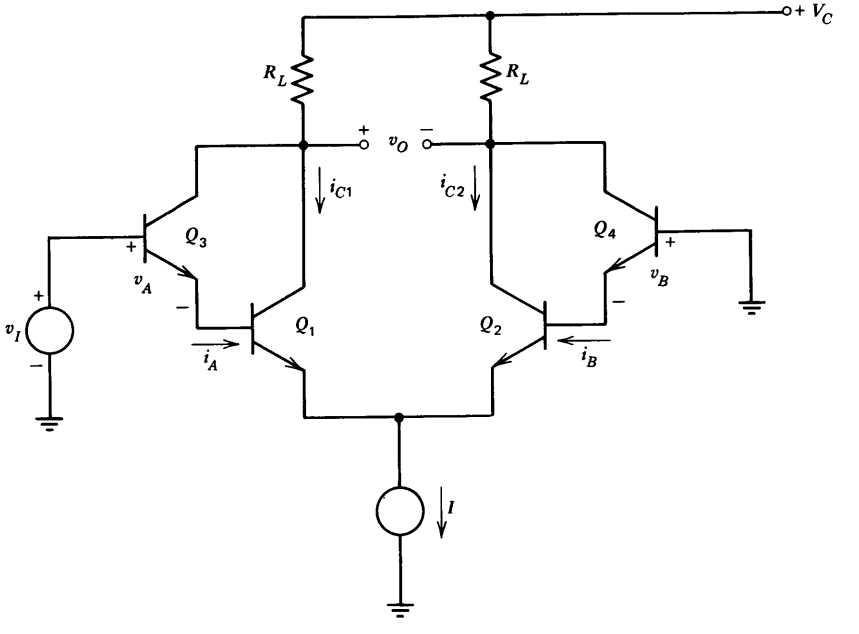


Figure 7.20 Differential amplifier with Darlington transistors.

Assume the operating point values for the two emitter currents are I_A and I_B. The incremental changes in these two currents that arise from changes in the current gains of transistors Q_1 and Q_2 are related to I_A and I_B by

$$i_a = -I_A \frac{\Delta\beta_1}{\beta_1} \tag{7.41a}$$

$$i_b = -I_B \frac{\Delta\beta_2}{\beta_2} \tag{7.41b}$$

where $\Delta\beta/\beta$ is recognized as the fractional change in current gain for a transistor.

The incremental output resistance of an emitter follower is approximately equal to the reciprocal of its transconductance. Thus the incremental differential change between v_A and v_B caused by changes in i_A and i_B, which is identically equal to the change in v_I required to keep v_O equal to zero is

$$v_a - v_b = \frac{i_a}{g_{m3}} - \frac{i_b}{g_{m4}} = \frac{I_B\Delta\beta_2}{g_{m4}\beta_2} - \frac{I_A\Delta\beta_1}{g_{m3}\beta_1} \tag{7.42}$$

Since the transconductances are proportional to operating-point currents, Eqn. 7.42 reduces to

$$v_a - v_b = \frac{I_B\Delta\beta_2}{(qI_B/kT)\beta_2} - \frac{I_A\Delta\beta_1}{(qI_A/kT)\beta_1} = \frac{kT}{q}\left(\frac{\Delta\beta_2}{\beta_2} - \frac{\Delta\beta_1}{\beta_1}\right) \tag{7.43}$$

Note that the drift component attributable to this effect is dependent only on the differential changes in the fractional current gains of the inner transistors. A typical value for the fractional change in current gain with temperature is 0.6% per degree Centigrade. If transistors Q_1 and Q_2 have this value matched to within 10%,[17] the resultant drift is 15 μV/°C.

Another potential difficulty with the use of the Darlington input connections is that its fractional change in input current with temperature is approximately a factor of two greater than that of an individual transistor because two devices are cascaded in the Darlington connection. Thus the low bias current of the Darlington configuration does not result in correspondingly low changes in bias current with temperature.

It is possible to trade input current for drift by increasing the emitter currents of Q_3 and Q_4 above the base currents of Q_1 and Q_2, for example

[17] This degree of match is realistic for discrete transistors selected for matched base-to-emitter voltages and current gains. Better results are normally achieved with monolithic matched transistors where the manufacuring process for the two devices is highly uniform.

by placing resistors from base to emitter of Q_1 and Q_2. Changes in base current have less effect since the output resistances of Q_3 and Q_4 are lower as a consequence of increased bias current. This technique is frequently used in the design of amplifiers with Darlington input transistors.

7.5 DRIFT CONTRIBUTIONS FROM THE SECOND STAGE

Thus far the discussion has focused on single-stage direct-coupled amplifiers. No consideration has been given to situations that require a second stage either to provide greater voltage gain or to isolate a low-resistance load. The use of a second stage is mandatory in the design of operational amplifiers and thus must be investigated.

There is a popular misconception that the dominant source of voltage drift for a d-c amplifier is always associated with its input stage. The argument supporting this view is that drift arising in the second stage is divided by the gain of the first stage when referred to the input of the amplifier, and is negligible if the first-stage gain is high. This assumption is not always justified because of the extraordinarily low values of drift that can be achieved with a properly balanced first stage. Balancing techniques similar to those used for the input stage are not effective for the second stage, since its drift contribution is often attributable to variations in input current rather than in base-to-emitter voltage.

7.5.1 Single-Ended Second Stage

Figure 7.21 shows a differential first stage (with two matched transistors collectively labeled Q_1) driving a common-emitter PNP second stage. Two perturbation sources are shown, which will be used later to calculate drift. In addition to providing gain, the second stage shifts level so that the output voltage can swing both positive and negative with respect to ground. If the base resistance of all transistors is negligibly small, the voltage gain of this amplifier is

$$\frac{v_o}{v_i} = \frac{-g_{m1}R_{L1}\beta_2 R_{L2}}{2(r_{\pi 2} + R_{L1})} \tag{7.44}$$

Drift referred to the input for this two-stage amplifier is calculated as before by determining how v_I must vary to keep v_O equal to zero. Note that in order to maintain a fixed output voltage, it is necessary for i_{C2} to remain constant. There are a number of sources of drift for this amplifier. In this development only changes in i_{B2} and v_{EB2} that arise as the parameters of Q_2 vary are considered. These changes can be modeled by the perturbation generators shown in Fig. 7.21. If the changes are small compared

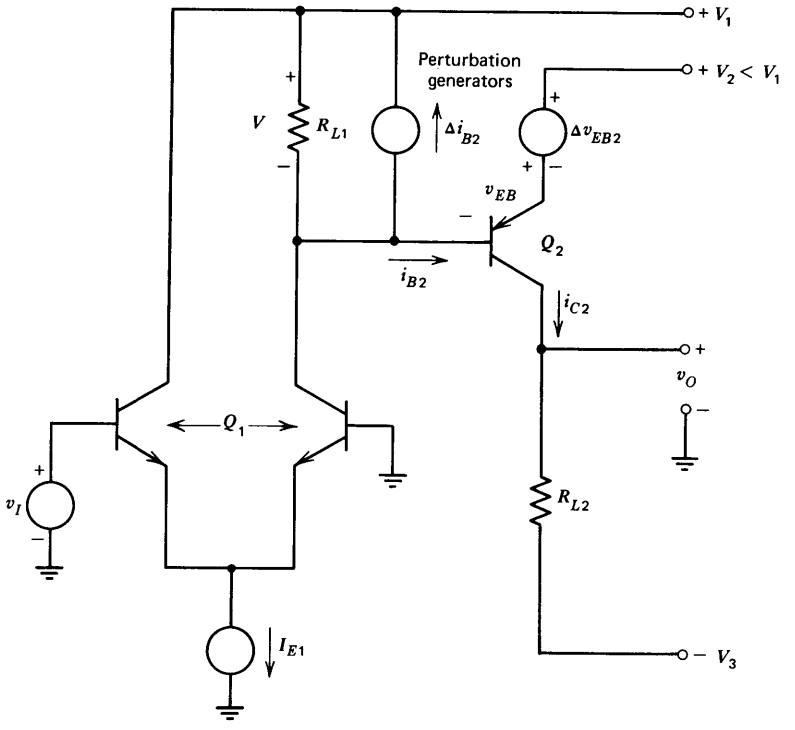


Figure 7.21 Two-stage d-c amplifier.

to operating-point values, linear analysis methods can be used to determine the drift referred to the input of the amplifier.

The results of this analysis show

$$v_I\Big|_{i_{C2}\,=\,\text{const}} = \frac{-2\,\Delta v_{EB2}}{g_{m1}R_{L1}} - \frac{2\,\Delta i_{B2}}{g_{m1}} \tag{7.45}$$

The gain portion of the first term on the right of Eqn. 7.45 can be expressed in terms of V, the quiescent voltage across R_{L1}. Similarly, the second term can be expressed in terms of I_{E1}, I_{C2}, the current gain of Q_2, and its fractional change. These substitutions yield

$$v_I\Big|_{i_{C2}\,=\,\text{const}} = \frac{-2kT\,\Delta v_{EB2}}{qV} + \frac{4kTI_{C2}\,\Delta\beta_2}{qI_{E1}\beta_2^2}$$

$$\simeq \frac{-\Delta v_{EB2}}{20V} + \frac{I_{C2}\,\Delta\beta_2}{10I_{E1}\beta_2^2} \tag{7.46}$$

at room temperature.

Typical values are used to illustrate magnitudes of these drift components with temperature. The voltage V is constrained by available supply voltages, and a value of 5 volts is assumed. The typical Δv_{EB} value of -2 mV/°C is used. A current gain of 300 coupled with a temperature coefficient of 0.6% per degree Centigrade is assumed for Q_2. Because the quiescent current level normally increases from the first stage to the second, a ratio of 5 is used for I_{C2}/I_{E1}. Substituting these values into Eqn. 7.46 shows that the drift attributable to changes in v_{EB2} is approximately 20 μV/°C, while the component arising from i_{B2} changes is 10 μV/°C. These values contrast dramatically with the drift that can be obtained from a properly designed first stage, and indicate the dominant effect that the second stage can have on drift performance.

The drift calculations of this section apply even if current gain only is required from the second stage. It is easy to show that the calculated values of drift are the same if an emitter follower is used in place of the grounded-emitter stage.

The final term in Eqn. 7.46 indicates the importance of changes in second-stage input current on drift performance. This term indicates that the drift performance deteriorates as the ratio of the quiescent operating current of the second stage to that of the first stage is increased. This result is one example of how certain design considerations (in particular, the desire to increase quiescent currents from the first to subsequent stages) must be compromised to achieve low drift performance.

7.5.2 Differential Second Stage

It is evident from the typical values calculated in the last section that unless care is taken in the design of the second stage of a d-c amplifier, this stage can easily dominate the drift performance of the circuit. One approach to the design of low-drift multistage d-c amplifiers is to use a differential second stage so that reflected drift is determined by differential rather than absolute changes in second-stage parameters.

Figure 7.22 shows a two-stage differential amplifier. Individual members of the first- and second-stage pairs are assumed matched. It is further assumed that a single-ended output is desired, so one collector of the second-stage pair is grounded.

Normally a resistor is used in place of the current source I_{E2}. Since only differential input signals can be applied to the second stage, and therefore the common-emitter point of the second stage is incrementally grounded, the impedance connected to this point is irrelevant. However, the calculations are somewhat more convenient if a current source is included.

It is interesting to note that the voltage gain of this amplifier is identical to that of Fig. 7.21. Since the common-emitter connection of the second

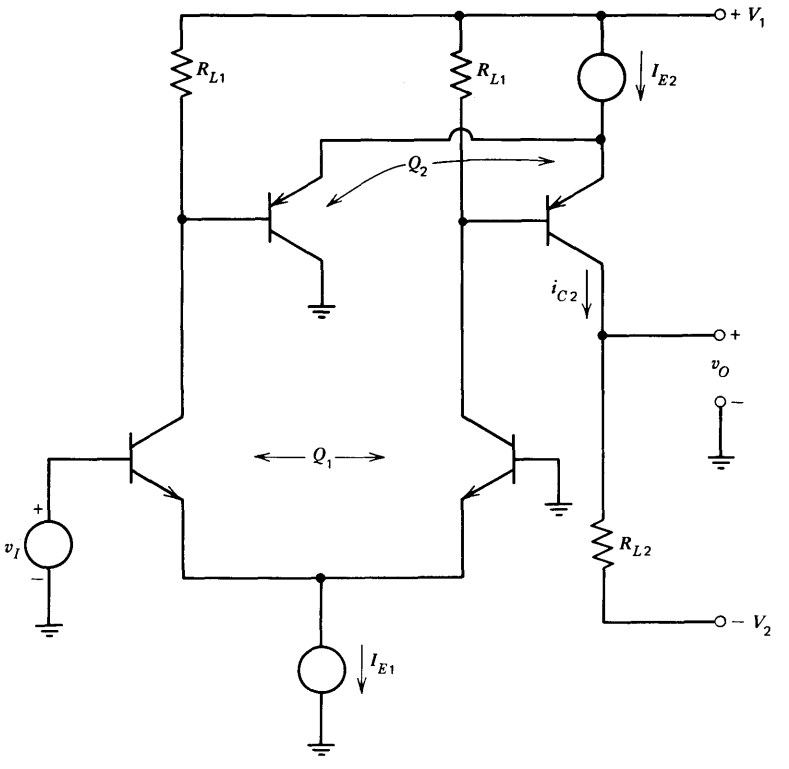


Figure 7.22 Amplifier with two differential stages.

stage is incrementally grounded for any possible input signal, no gain increase results from the left-hand member of the PNP pair.

Input drift attributable to second-stage differential base-to-emitter voltage changes is generally negligible if any degree of match exists. The drift referred to the input of the second stage is equal to the ratio $\Delta v_{BE2}/T$ per degree Centigrade (see Section 7.3.4). This value (typically on the order of 10 to 100 μV/°C) is divided by the unloaded differential voltage gain of the first stage (twice the single-ended value calculated in the preceding section) when reflected to the input.

The drift attributable to differential fractional changes in second-stage current gain is (assuming initially matched values for second-stage current gains)

$$v_I \Big|_{i_{C_2} = \text{const}} = \frac{kTI_{E2}}{\beta_2 q I_{E1}} \left(\frac{\Delta\beta_{2A} - \Delta\beta_{2B}}{\beta_2} \right) \tag{7.47}$$

where the A and B subscripts indicate the two members of the second-stage pair. (The factor of four compared with the calculation of the last section occurs since each second-stage transistor is operating at $I_{E2}/2$ and since the differential connection requires that only half the differential current change be offset at either side.) The quantity $(\Delta\beta_{2A} - \Delta\beta_{2B})/\beta_2$ is typically 0.1% per degree Centigrade for well-matched discrete components, and is often lower for integrated-circuit pairs. It is interesting to note that this component of drift dominates many amplifier designs, particularly if the current gains and the temperature coefficients of the second stage are not well matched, or if the operating current level of the second stage is high relative to that of the first stage.

The use of a Darlington second stage with its lower input current offers some improvement, since the higher voltage drift of the Darlington is tolerable in this stage. Another possibility is to adjust the relative collector currents of the second stage so that the differential change in second-stage base current with temperature is zero. Unfortunately, this adjustment is difficult to make.

7.6 CONCLUSIONS

The successful design of low-drift direct-coupled amplifiers depends on exploiting the unique tracking properties of the differential amplifier, and the application of a number of drift reducing tricks that have evolved. In view of the many possible pitfalls, it is reassuring to realize that the drift of several commercially available integrated-circuit operational amplifiers is on the order of 3 μV per degree Centigrade or lower, and that at least one discrete-component design achieves a drift of 0.5 μV per degree Centigrade.

The purpose of the simple but somewhat tedious derivations and examples of this section has not been to permit exact evaluation of the drift of a circuit, but rather to emphasize that "little things mean a lot," and to indicate the dominant drift sources of a particular design so that they may be reduced.

PROBLEMS

P7.1

Figure 7.23 shows several amplifying connections that consist of ideal amplifiers and passive components. Offset sources are shown as batteries. Calculate the offset referred to the input (the input voltage required to make $v_O = 0$), the output offset (the output voltage with $v_I = 0$), and the gain (v_o/v_i) for each connection.

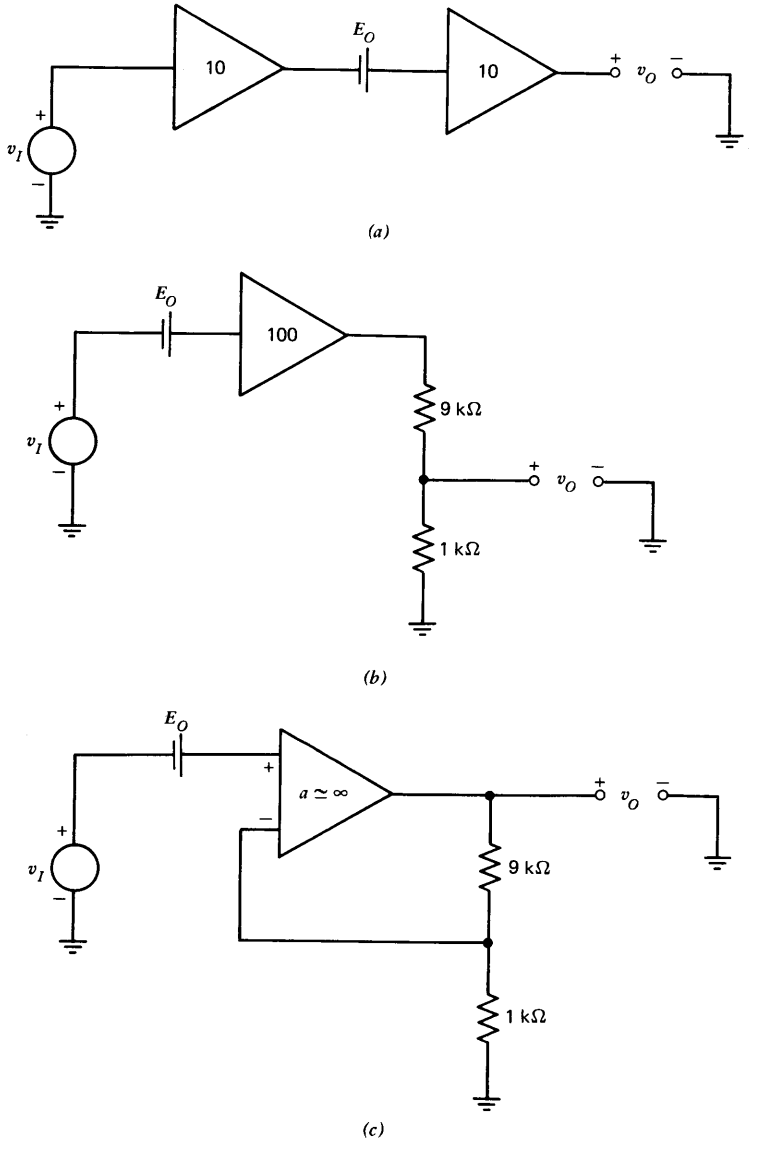
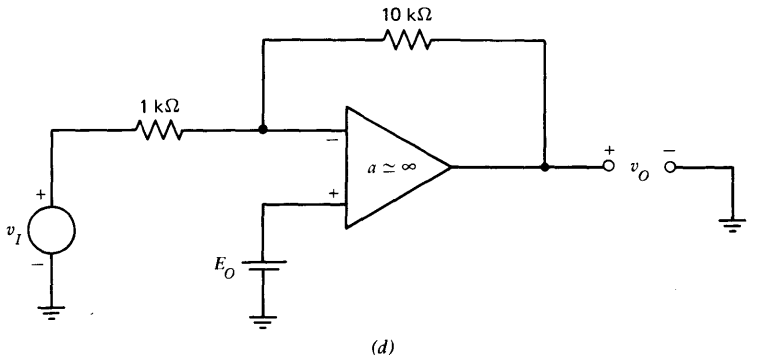
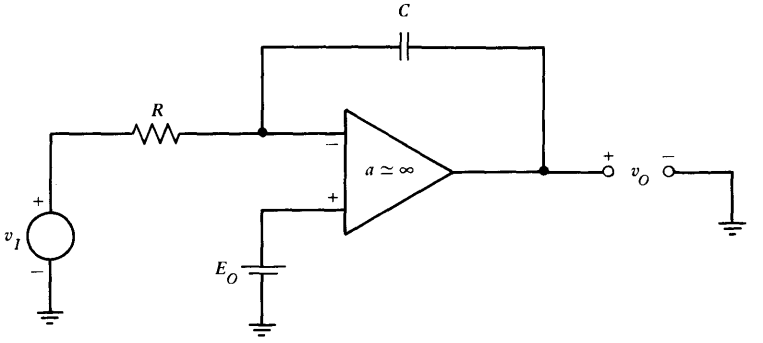


Figure 7.23 Amplifier Connections.



(d)



(e)

Figure 7.23—Continued

P7.2

Consider an operational amplifier with a particular value of offset E_O referred to its input. Compare the offset referred to the input of amplifier connections that combine this amplifier with passive components to provide inverting or noninverting gains with a magnitude of A.

P7.3

Figure 7.24 shows a circuit that can provide a temperature-independent output voltage. Assume that the transistor has very high β and that $i_O = 0$. The diode variables are related as

$$i_D = A_d T^3 \, e^{q(v_D - 0.782)/kT}$$

while the transistor relationship is

$$i_C = A_t T^3 \, e^{q(v_{BE} - 1.205)/kT}$$

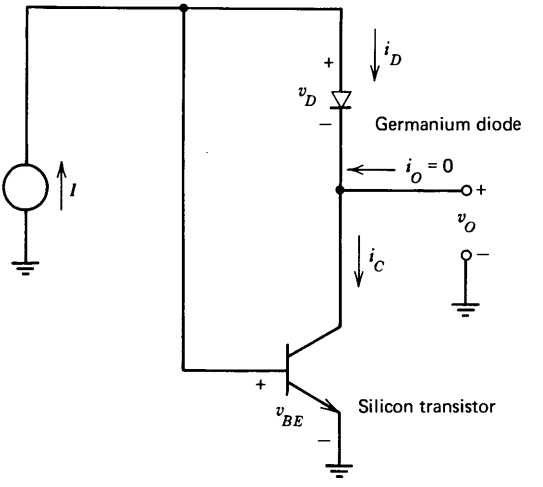


Figure 7.24 Voltage reference.

(a) For what ratio of A_d to A_t does $\partial v_O/\partial T = 0$?
(b) What is v_O with the condition of part *a* satisfied?
(c) What is the output resistance of this connection?

P7.4

The current-voltage relationship for a family of diodes can be approximated as

$$i_D = K\, e^{q(v_D - 1.2)/kT}$$

where K is a (temperature-independent) constant that may vary from diode to diode.

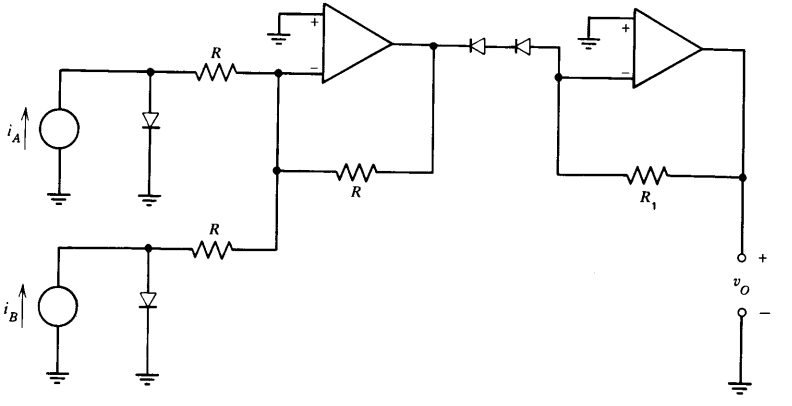


Figure 7.25 Nonlinear circuit.

(a) Four of these diodes with identical values for K are connected as shown in Fig. 7.25. Find v_O as a function if i_A and i_B. You may assume that the currents through all resistors R are much smaller than i_A or i_B and that both operational amplifiers are ideal.

(b) Determine an expression for

$$\left.\frac{\partial v_D}{\partial T}\right|_{i_D = \text{const}} \text{ for these diodes.}$$

(c) Assume that, because of incredibly poor control of the process used to make these diodes, it is possible to find two diodes which, at $T = 300°$ K and 1 mA of forward current, have forward voltages of 0.3 V and 0.9 V, respectively. These diodes are connected as shown in Fig. 7.26, and the pot is adjusted so that $\partial v_O/\partial T = 0$. What is v_O with this pot setting?

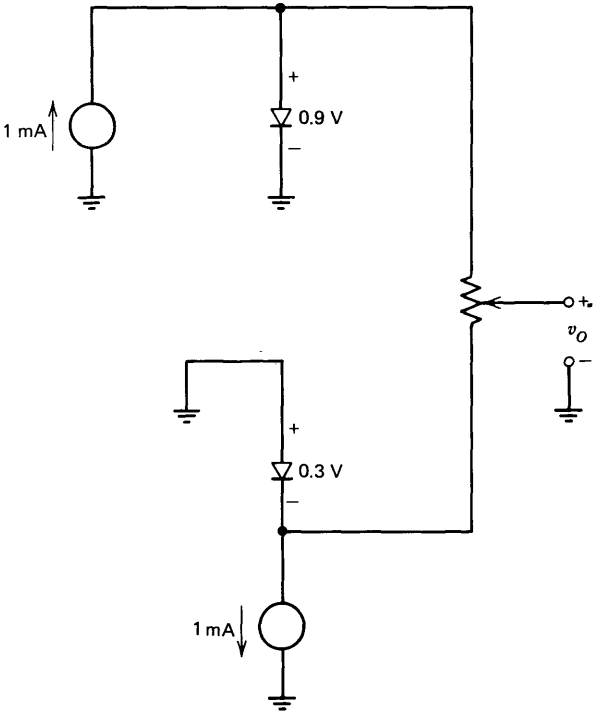


Figure 7.26 Voltage reference.

P7.5

The current-voltage relationship for a particular diode is

$$i_D = AT^{2.5}e^{q(v_D-1.205)/kT}$$

The value of the constant A is such that at 300° K and $v_D = 0.6$ V, $i_D = 1$ mA.

(a) Determine $\left.\dfrac{\partial v_D}{\partial T}\right|_{i_D = \text{const}}$

(b) Seven identical diodes are connected as shown in Fig. 7.27. By appropriate choice of i_B, it is possible to make v_O temperature independent over a limited range of temperature. Determine the required value of v_O so that

$$\left.\frac{\partial v_O}{\partial T}\right|_{i_B = \text{const}} = 0 \qquad \text{at } T = 300° \text{ K}$$

Approximate the value of I_B necessary to obtain the required value of v_O.

(c) Calculate the second derivative of v_O with respect to temperature. Use this value to estimate the temperature range over which v_O remains within one part in 10^5 of its 300° K value.

(d) Repeat part *b* assuming that the magnitude of the right-hand current source is increased to 10 mA.

The type of voltage reference that results from this topology is called a *band-gap reference*. The underlying principle is used as a voltage reference in several available integrated circuits.

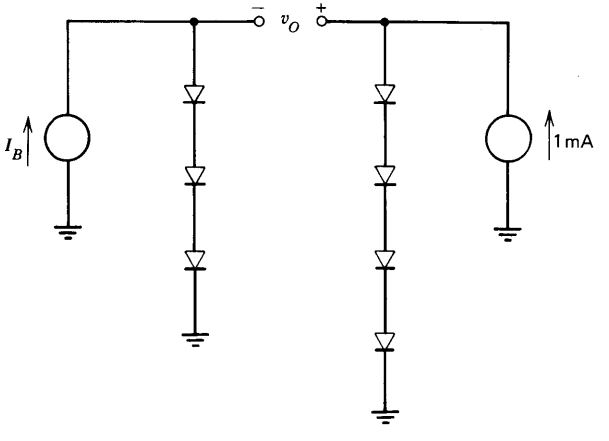


Figure 7.27 Band-gap standard.

P7.6

A differential amplifier is built with the topology shown in Fig. 7.11, with the exception that signals may also be applied to the base of the right-hand transistor. The value of the current source is 20 μA, and the incremental output resistance of this element is 10 MΩ. (The reasons for finite output resistance from current sources are discussed in Section 8.3.5.) Calculate the common-mode rejection ratio of this amplifier as a function the fractional unbalance in collector load resistors, Δ, assuming all transistor parameters are perfectly matched.

P7.7

An operational amplifier is built using a bipolar-transistor differential input stage. It is found that when the inverting input of the amplifier is grounded, the output voltage of the amplifier is zero at 25° C when a positive voltage of magnitude ΔV is applied to the noninverting input of the amplifier. You may assume that this offset and any temperature-dependent drift of the operational amplifier are caused only by a mismatch between the quantities I_S of the input-transistor pair, and that transistor variables are related by Eqn. 7.1.

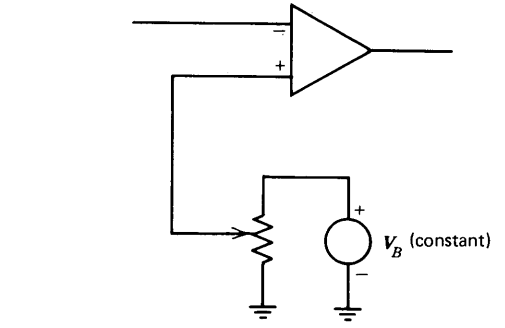
The operational amplifier is intended for use in an inverting-amplifier connection, and therefore it is possible to reduce the effective offset at the inverting input to zero at 25° C by applying a voltage ΔV to the noninverting input. Three techniques for obtaining this bias voltage are indicated in Fig. 7.28. Comment on the effectiveness of these three balancing methods in reducing the temperature drift of the amplifier. Assume that the diode forward-voltage variation with temperature is given by

$$\left.\frac{\partial v_D}{\partial T}\right|_{i_D = \text{const}} = \frac{(v_D - V_{go})}{T} - \frac{3k}{q}$$

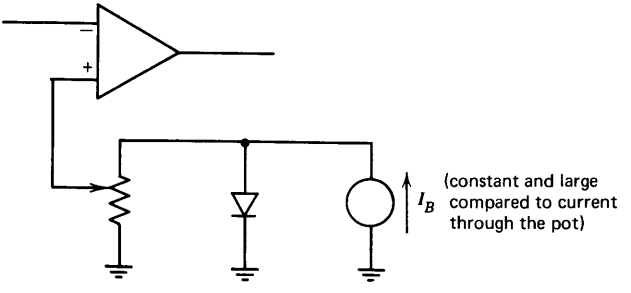
in parts *b* and *c*.

P7.8

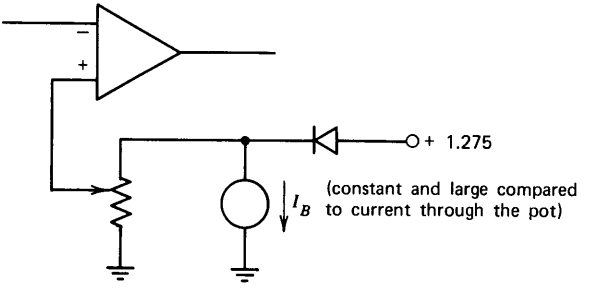
A differential amplifier is constructed and balanced as shown in Fig. 7.10. Following balancing, it is found that transistor Q_1 is operating at a quiescent collector current of 1.1 mA, while Q_2 operates at a collector current of 0.9 mA. The transistors used are discrete devices mounted in reasonably close thermal proximity, and have a differential thermal resistance of 20° C per watt (i.e., if one member of the pair operates at a power level ΔP watts above that of the other, its temperature is 20 $\times$ ΔP degrees Centigrade higher). Estimate the offset referred to the input that results for a one-volt change in power-supply voltage.



(a)



(b)



(c)

Figure 7.28 Methods to reduce offset at inverting terminal to zero. (Potentiometer set to make voltage at noninverting input ΔV at 300° K in all cases.)

P7.9

A differential amplifier that can provide low input capacitance, and, by proper control of bias voltage V_B, high common-mode rejection ratio, is shown in Fig. 7.29. Assume that Q_1 and Q_2 are perfectly matched. Further assume that $\beta_3 = \beta_4 = 100$ at 25° C. The output voltage is then zero for $v_I = 0$. Assume that the fractional change in β_3 is 0.5% per degree Centigrade, while that of β_4 is 1% per degree Centigrade. Calculate the offset referred to the input for a 1° C temperature change.

P7.10

An operational amplifier is found to have a bias-current requirement at its noninverting input that is 10% higher than that at its inverting input at all temperatures of interest. The amplifier is connected as shown in Fig. 7.30. Select the value of R that minimizes the effect of input current on circuit performance.

P7.11

The current at the inverting input of a certain operational amplifier is found to be equal to $10^{-3}A/T^2$ where T is the temperature in degrees Kelvin. The amplifier is to be used in an inverting connection; conse-

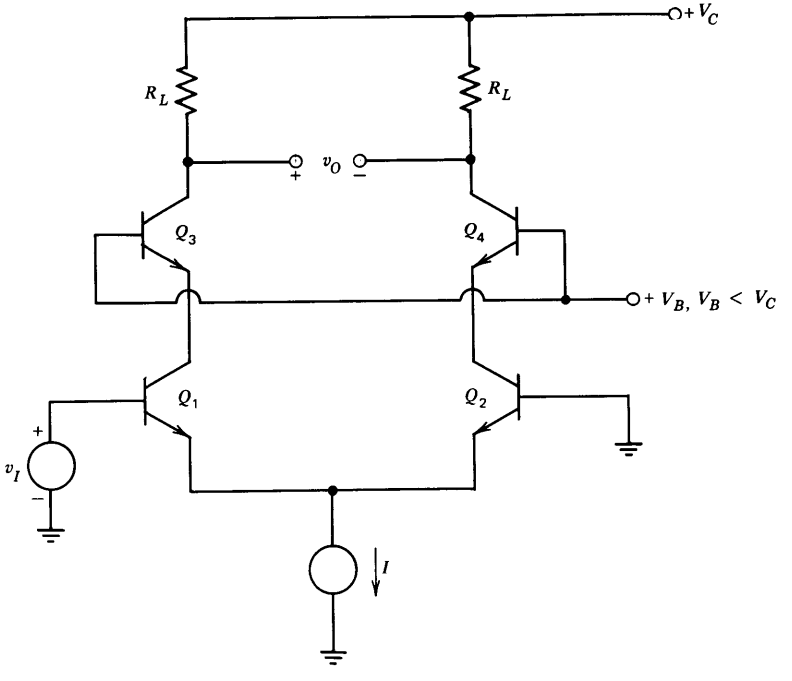


Figure 7.29 Cascoded differential amplifier.

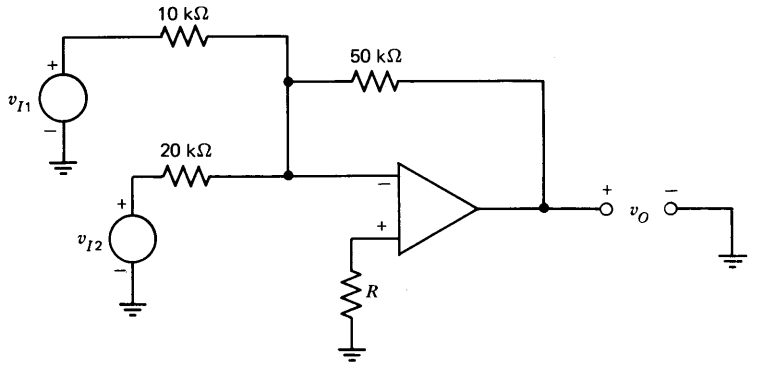


Figure 7.30 Summing amplifier.

quently the technique illustrated in Fig. 7.15 can be employed for input-current compensation. Parameters are selected so that the diode operates at a very nearly constant 1 mA, and its forward voltage at 300° K is 600 mV at this current. The diode current-voltage characteristics are of the general form

$$i_D = AT^3 e^{q(V_D - V_{g0})/kT}$$

Select resistor R_2 and bias source V_A in Fig. 7.15 so that the input current and its derivative with respect to temperature are cancelled at 300° K. What is the maximum compensated input current over the temperature range of 250 to 350° K using this form of compensation? Contrast this range with the corresponding quantity obtained with no compensation and by cancelling the input current at 300° K with a fixed bias current.

P7.12

The use of Darlington-connected input-stage transistors is discussed in Section 7.4.4. An alternative high-gain connection is the complementary Darlington connection shown in Fig. 7.31*a*. A differential amplifier employing this connection is shown in Fig. 7.31*b*. Determine the voltage drift of this connection as a function of relative current-gain changes of the Q_1-Q_2 pair by an argument similar to that used for Fig. 7.20.

P7.13

A regulated power supply is constructed as shown in Fig. 7.32. This supply uses feedback around a very simple d-c amplifier in an attempt to make $v_O = V_R$.

(a) Determine the output voltage for circuit values as shown.

(b) How much does the output voltage change for a small fractional change in the current gain of Q_2?
(c) Suggest a circuit modification that will reduce the dependence of v_O on the fractional change in β_2.

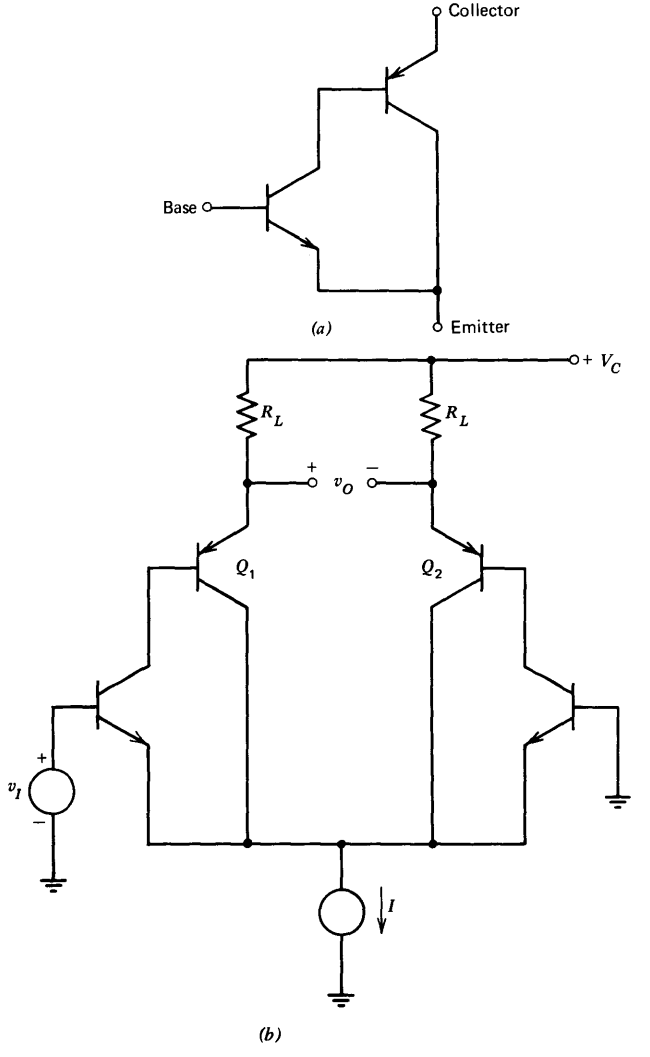


Figure 7.31 Differential amplifier using complementary Darlington-connected input transistors. (*a*) Base, collector, and emitter refer to terminals of the compound transistor. (*b*) Connection.

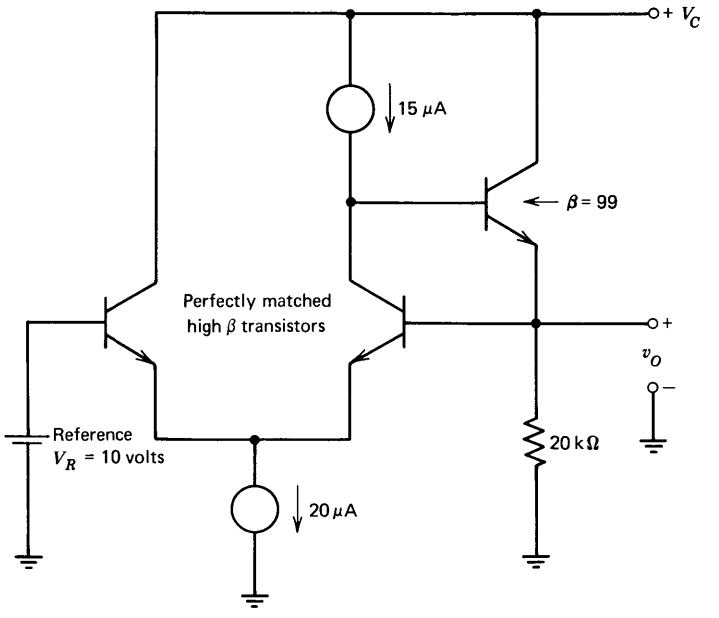


Figure 7.32 Power supply.

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