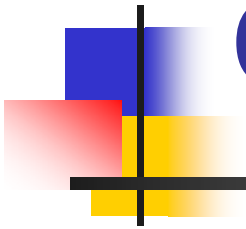


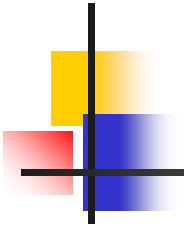
3.155J/6.152J Lecture 18: CMOS

Prof. Martin A. Schmidt

Massachusetts Institute of Technology

11/16/2005

Some of the slides in this presentation are from A. Akinwande (MIT) and G. May (Georgia Tech)

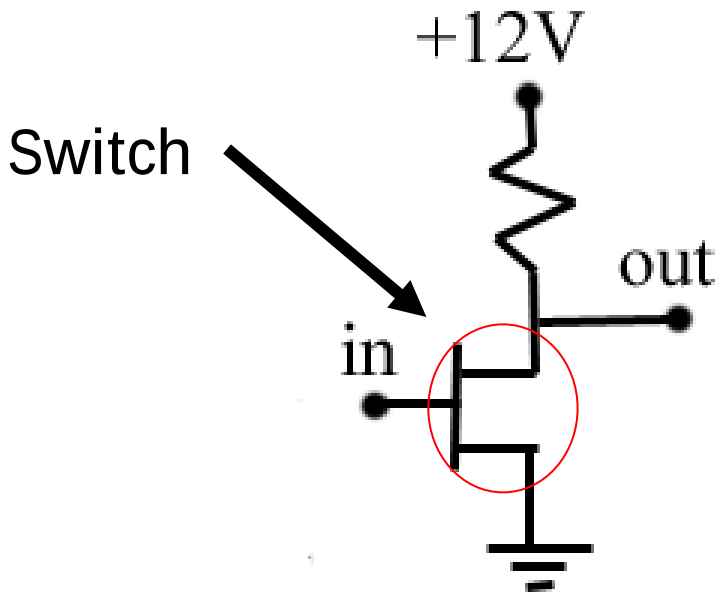


Outline

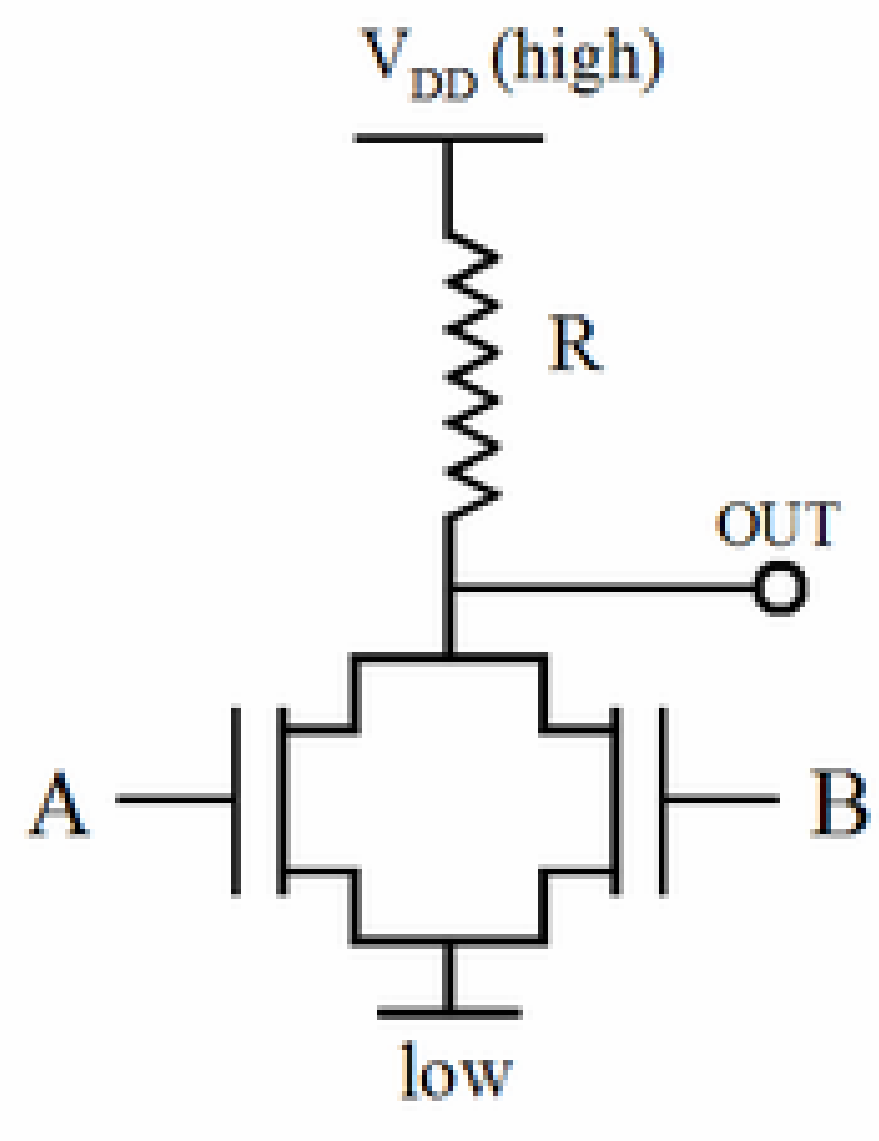
- Digital Logic
- Logic Technologies
  - Bipolar – TTL (Transistor-Transistor-Logic)
    - Comparatively higher power, but fast!
  - MOS
    - Very low power
    - Need in calculators, digital watches circa ~1975
  - MOS Technolgies
    - Metal Gate PMOS
    - Silicon Gate NMOS
      - E/D NMOS
    - CMOS
- CMOS Processes
- Reference: Plummer, Chapter 2

Digital Logic

- Fundamental Building Blocks
  - **Inverter**
  - NAND, NOR
  - Memory Cell
- Inverter
  - Switch Issues
    - Input current
    - Off-state leakage
    - On-state resistance

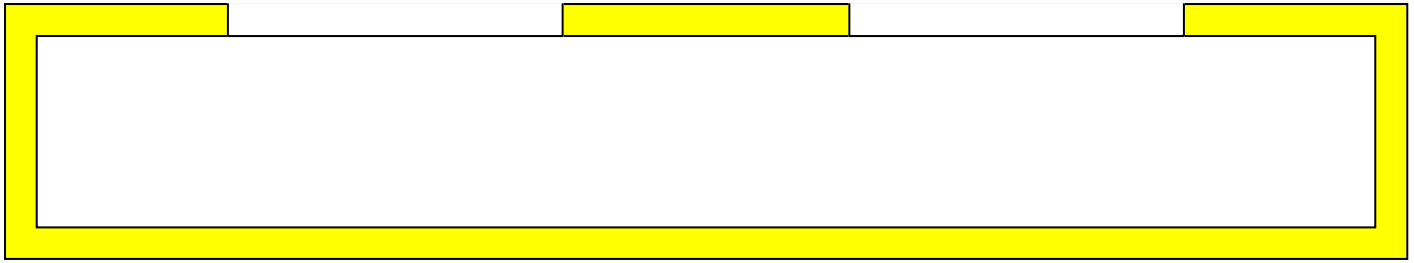


NOR Logic Gate



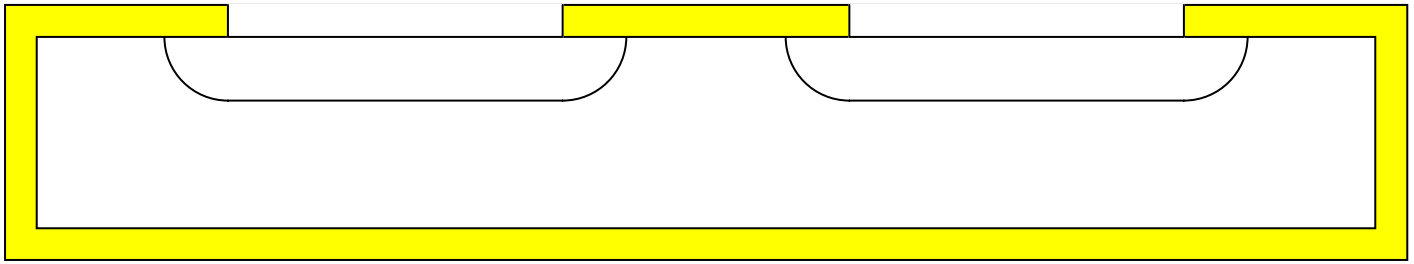
Metal Gate PMOS

Oxidation

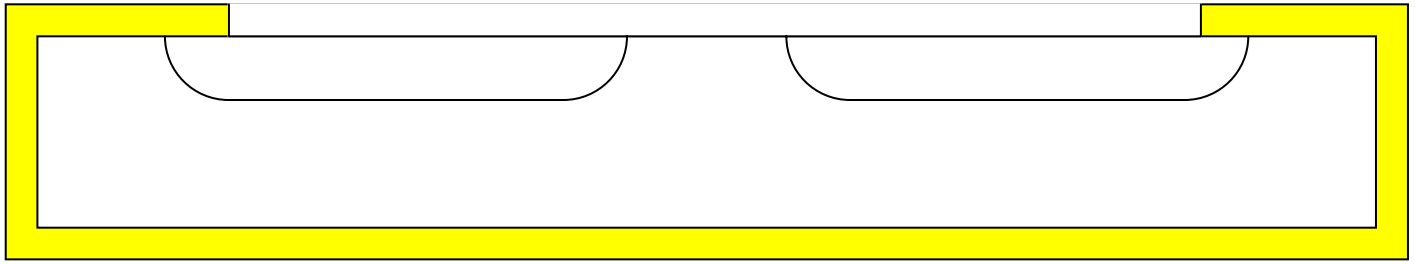


Source/Drain Photo

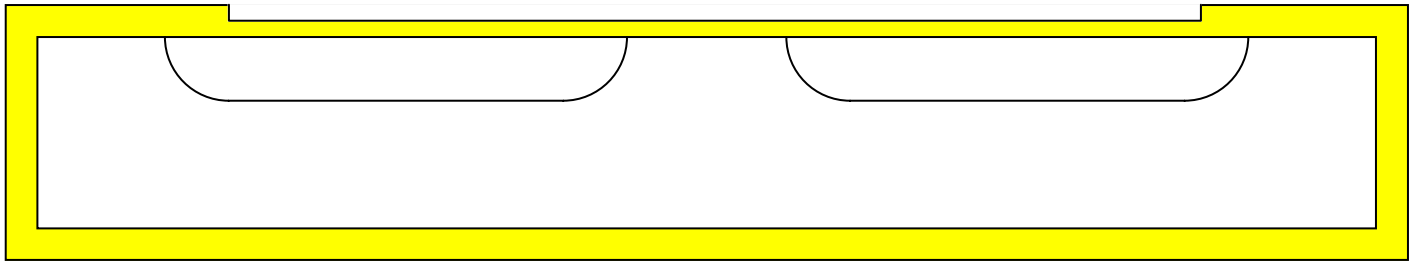
Metal Gate PMOS



S/D Diffusion (Solid Source)

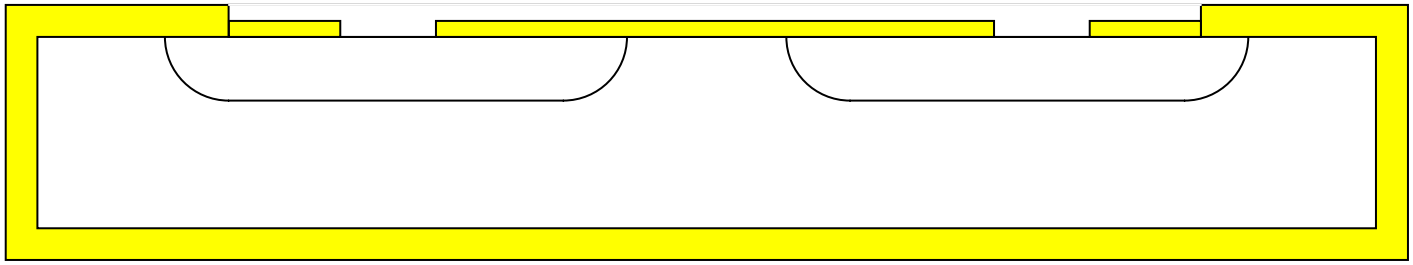


Clear Gate Region

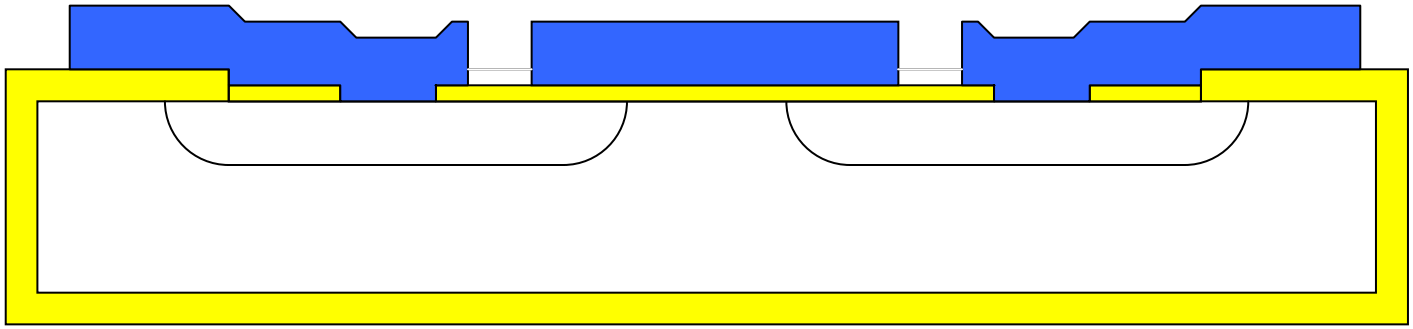


Gate Oxidation

Metal Gate PMOS



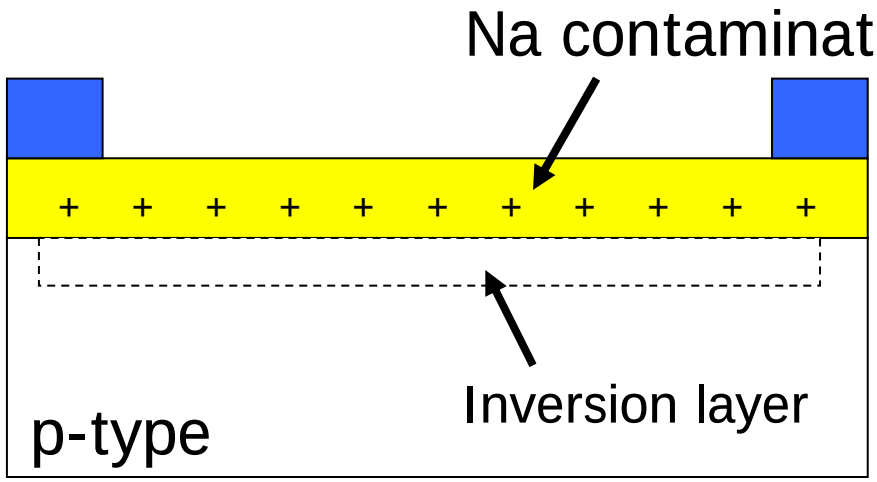
Open Contact Cuts



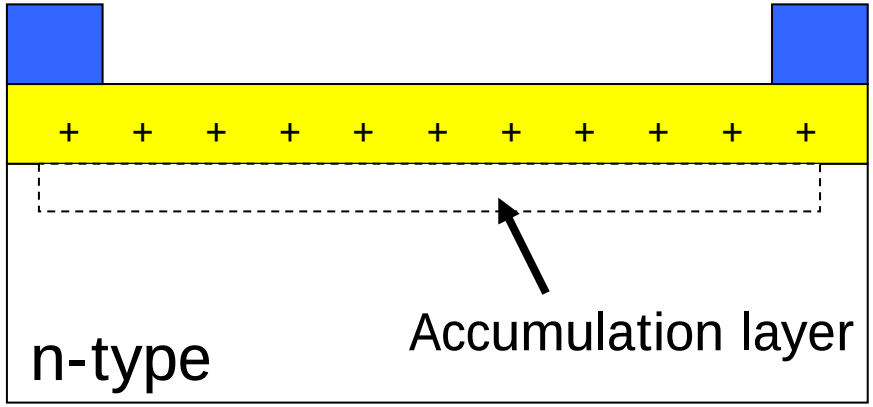
Metal

- Issues
  - Gate Overlap
  - Processing *after* gate oxidation

Why PMOS? – Field Inversion

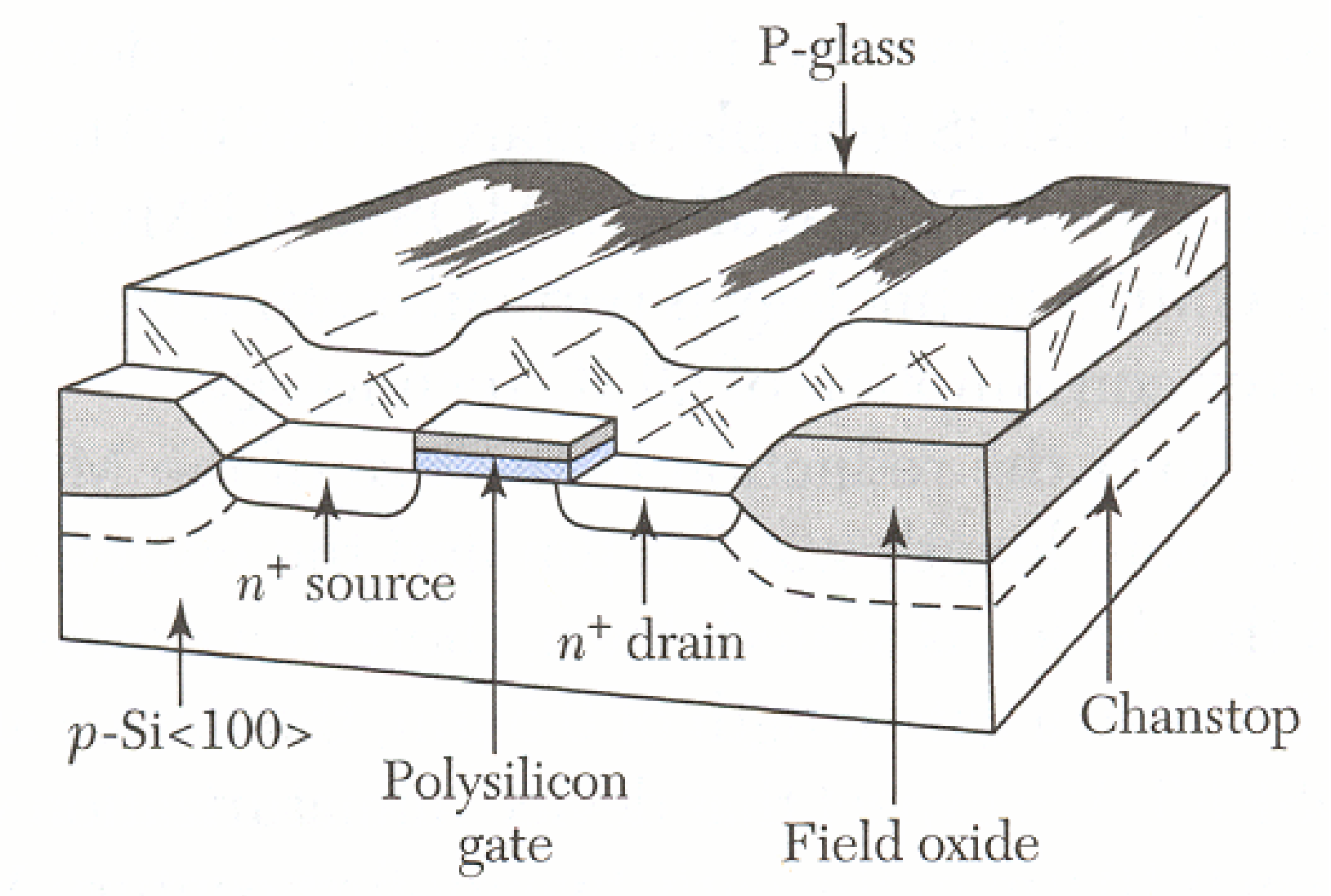


Shorts together adjacent devices



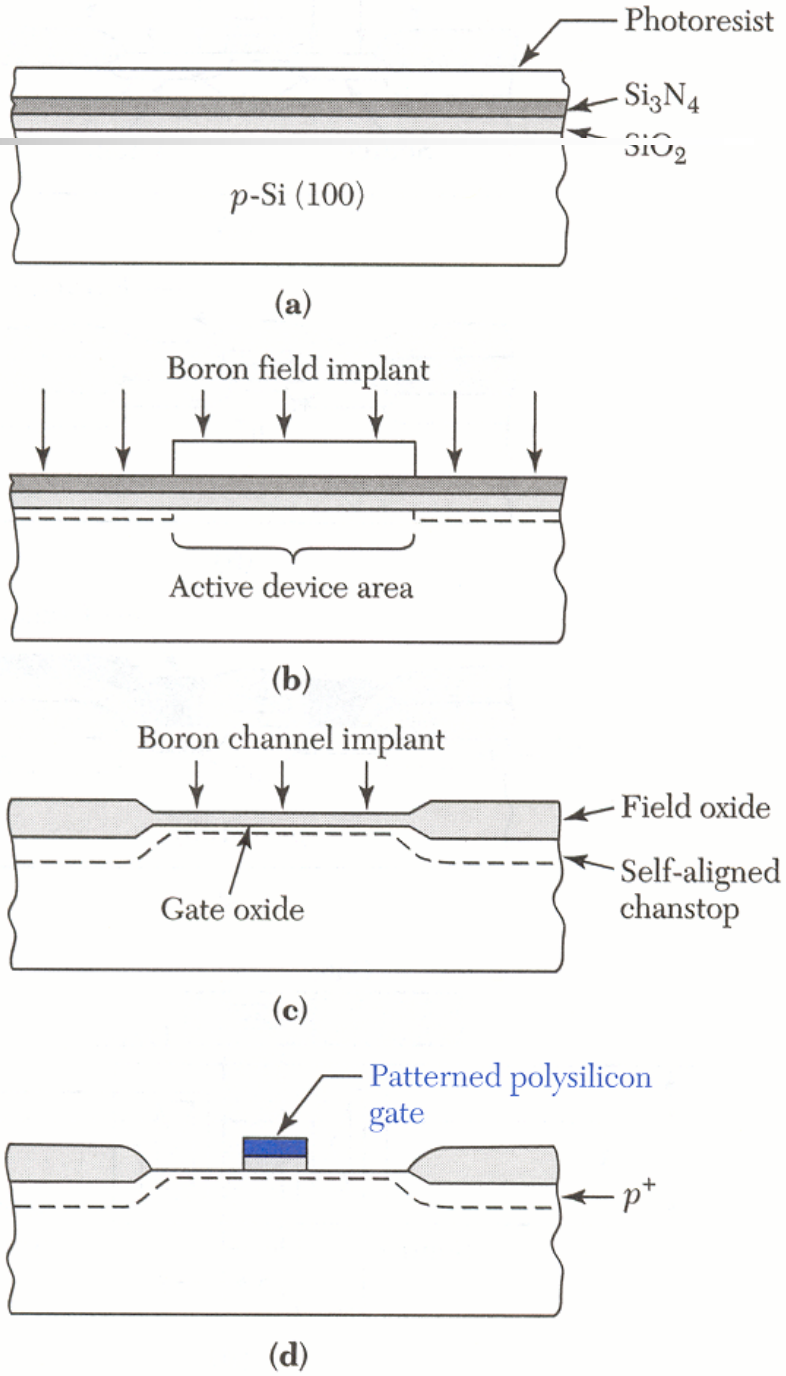
Devices remain isolated

Standard NMOS



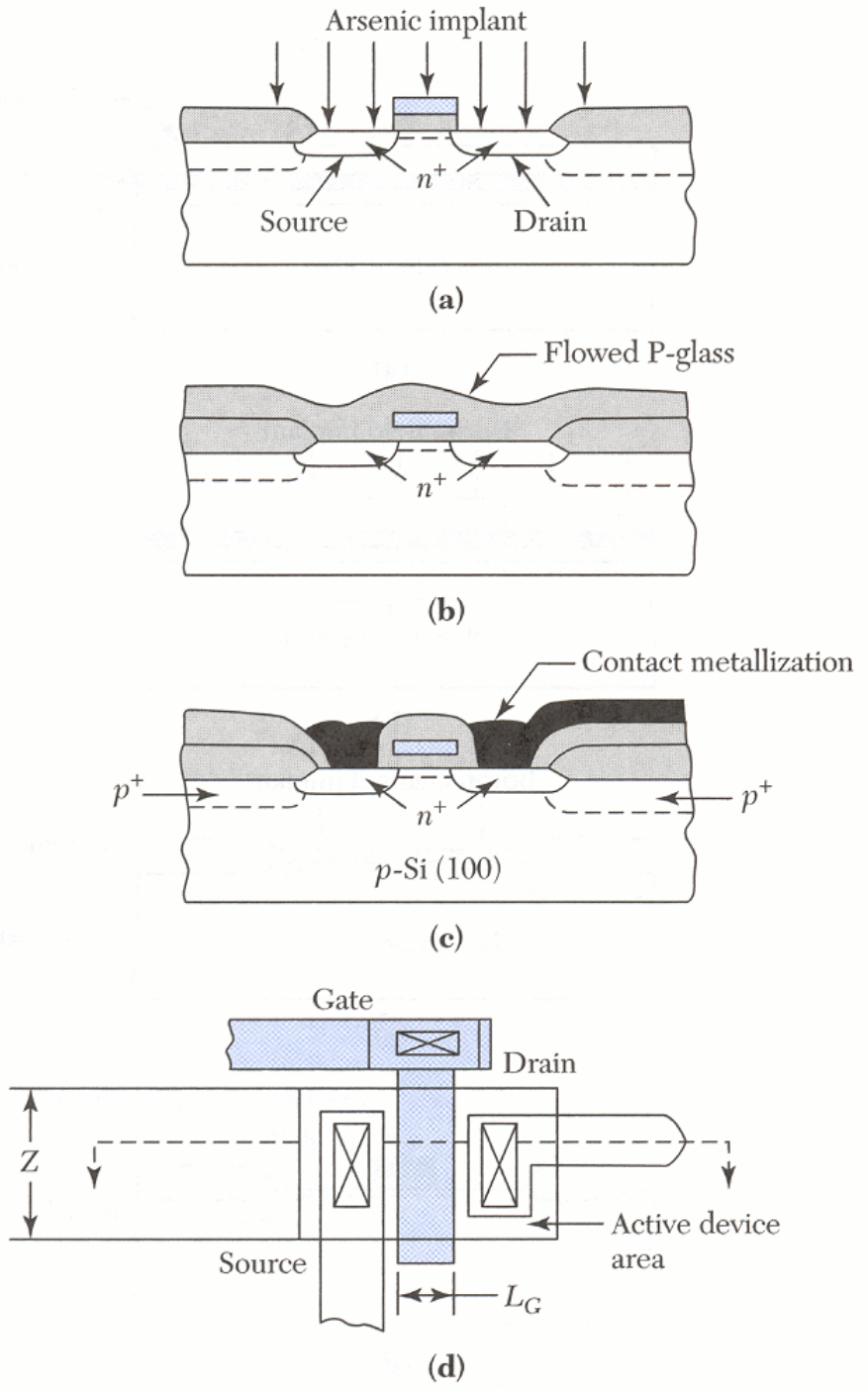
Process

- Start w/ p-type, lightly doped (~10^{15} cm^{-3}), <100>-oriented Si
- Form oxide isolation region (a)
- Define active area with photoresist mask and boron channel stop layer implanted through nitride-oxide layer (b)
- Grow gate oxide (< 10 nm) and adjust threshold voltage by implanting B ions (enhancement-mode device) (c)
- Form gate by depositing doped polysilicon. Pattern gate in source and drain regions (d)



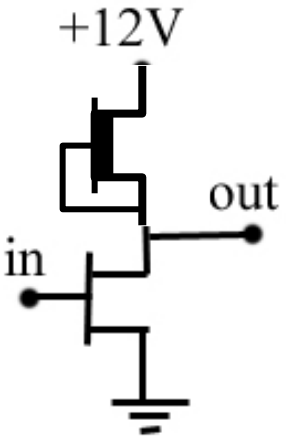
Process(cont.)

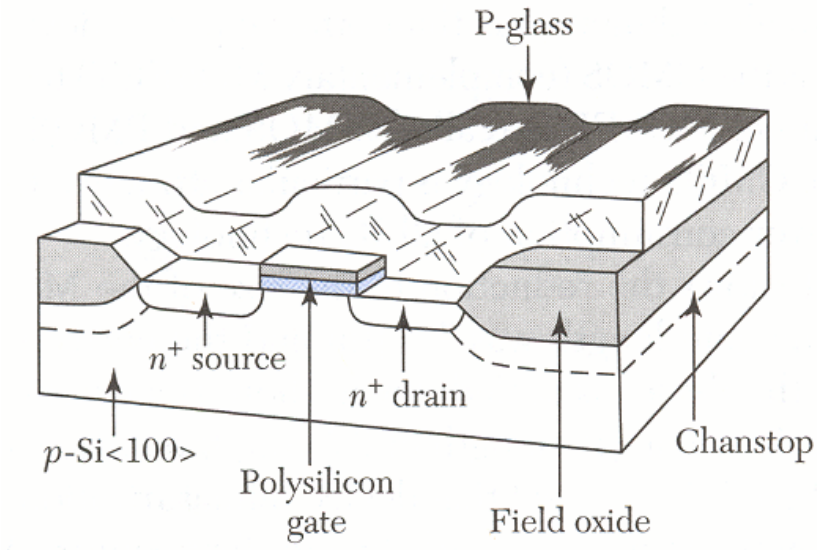
- Implant arsenic (~30 keV, ~5 × 10^{15} cm^{-2}) to form source and drain (a)
- Phosphorous-doped glass deposited and flowed (b)
- Contact windows defined and etched in P-glass. Al is deposited and patterned (c)
- Top view of completed MOSFET (d)



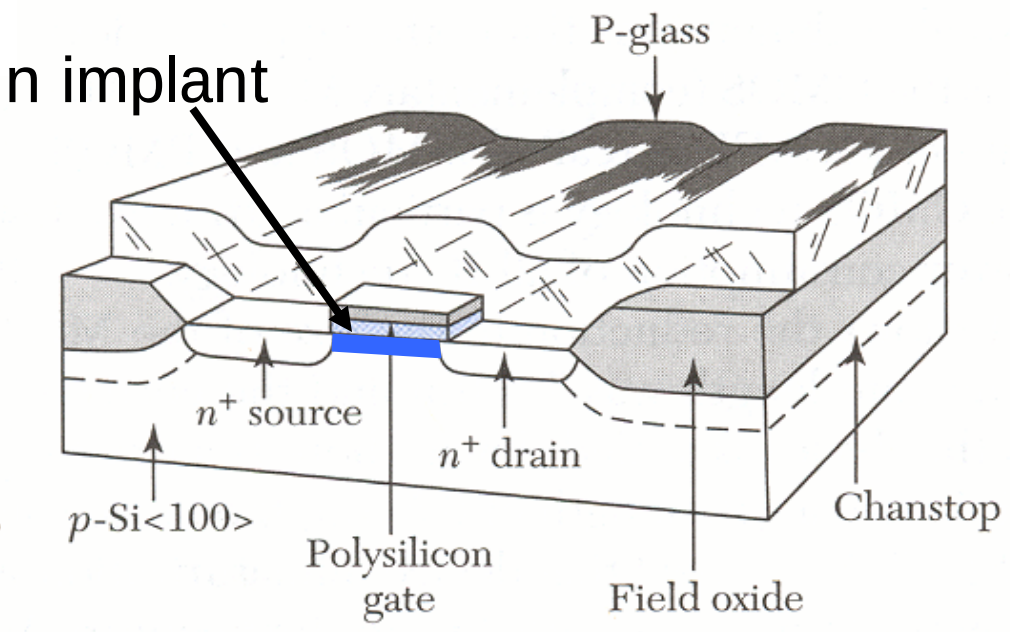
E/D NMOS Inverter

- Replace resistor with an ‘always on’ MOS
  - channel implant (requires one additional mask)





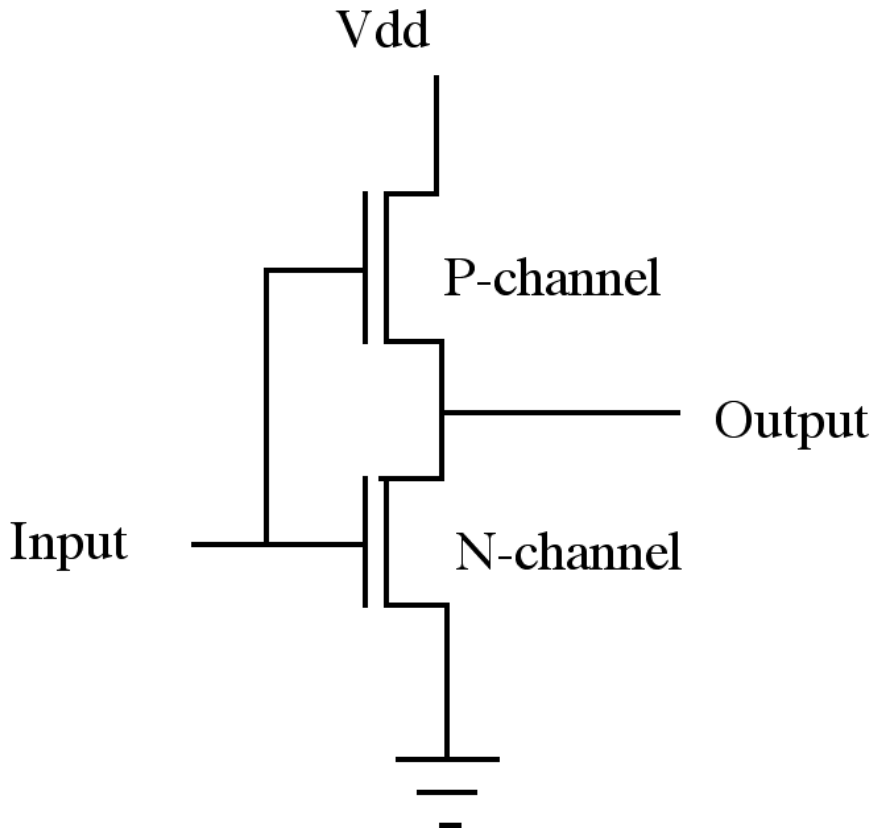
Enhancement Device



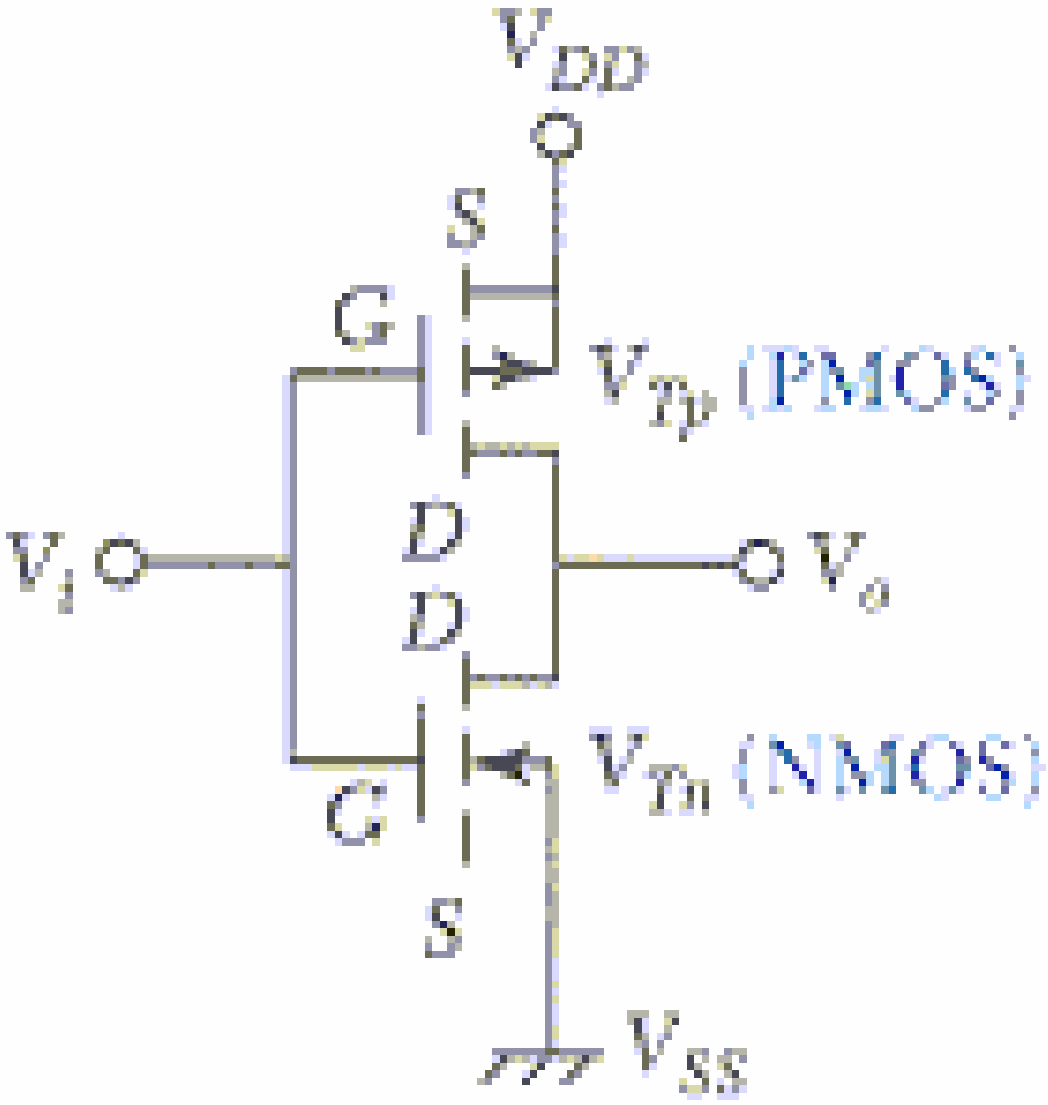
Depletion Device

CMOS Inverter Schematic

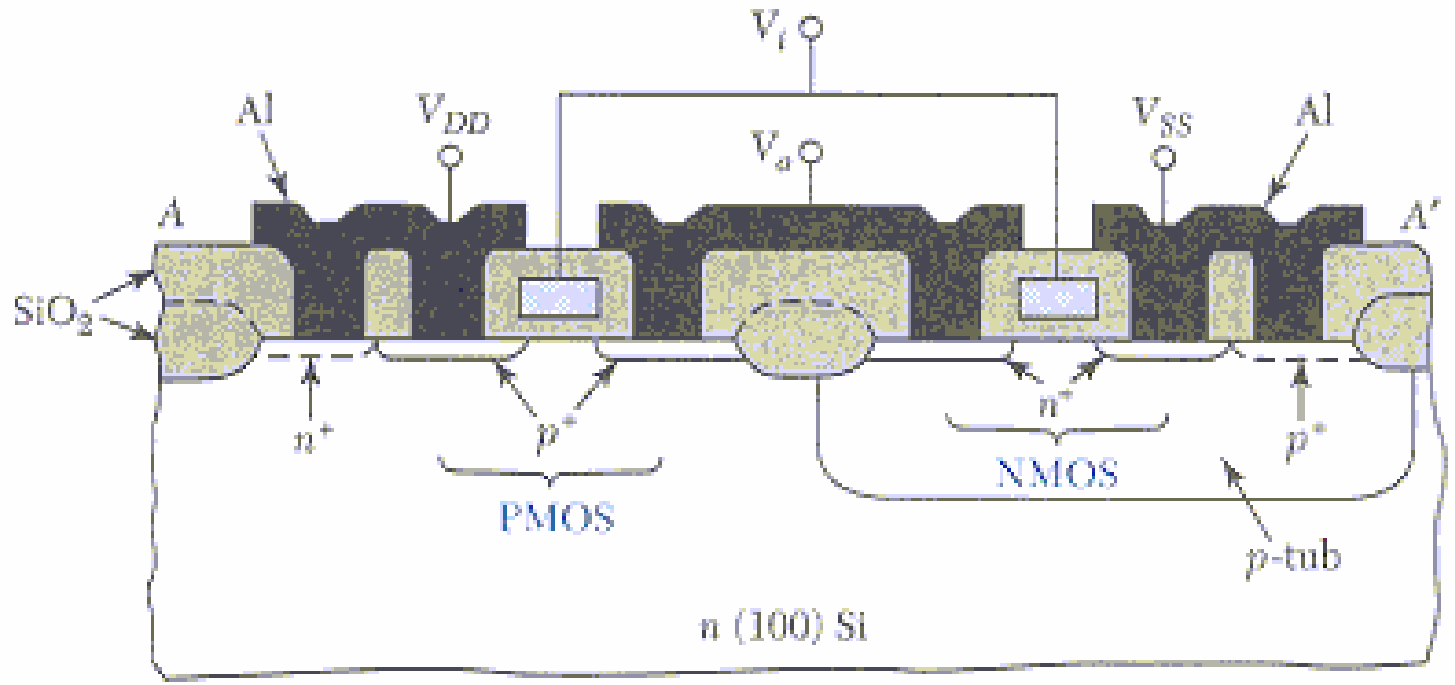
- Gate of upper PMOS device connected to the gate of lower NMOS device.
- Functions as a digital switch
- Low power consumption (~ nW) is most attractive feature



CMOS Inverter (w/ bulk contacts)

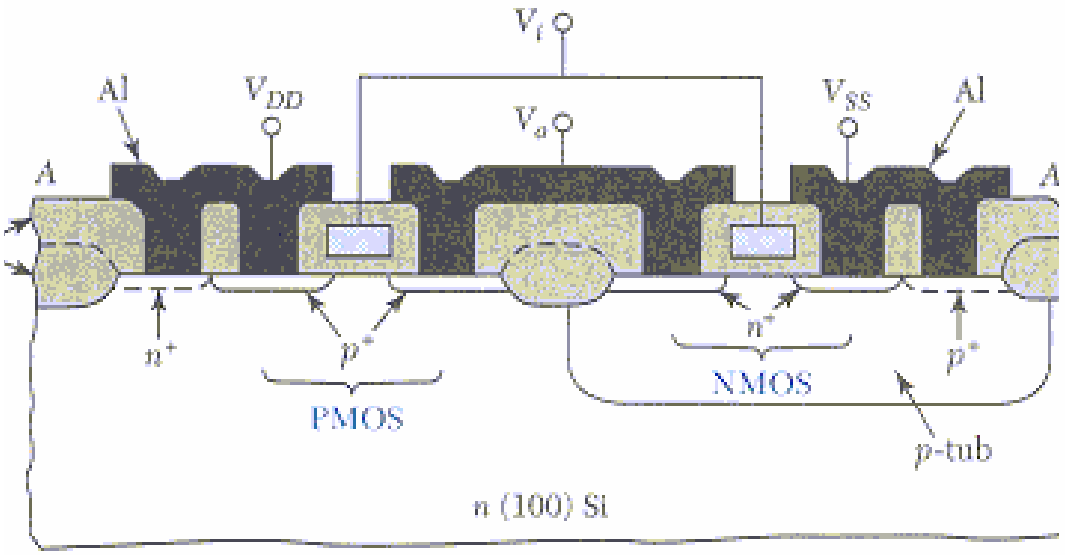


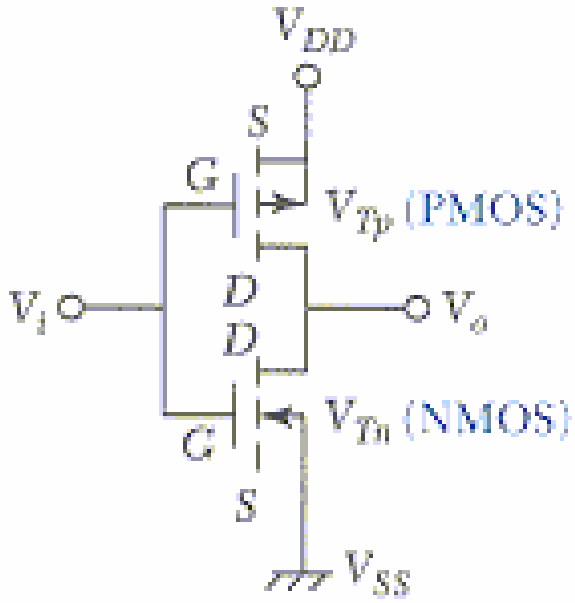
CMOS Processing

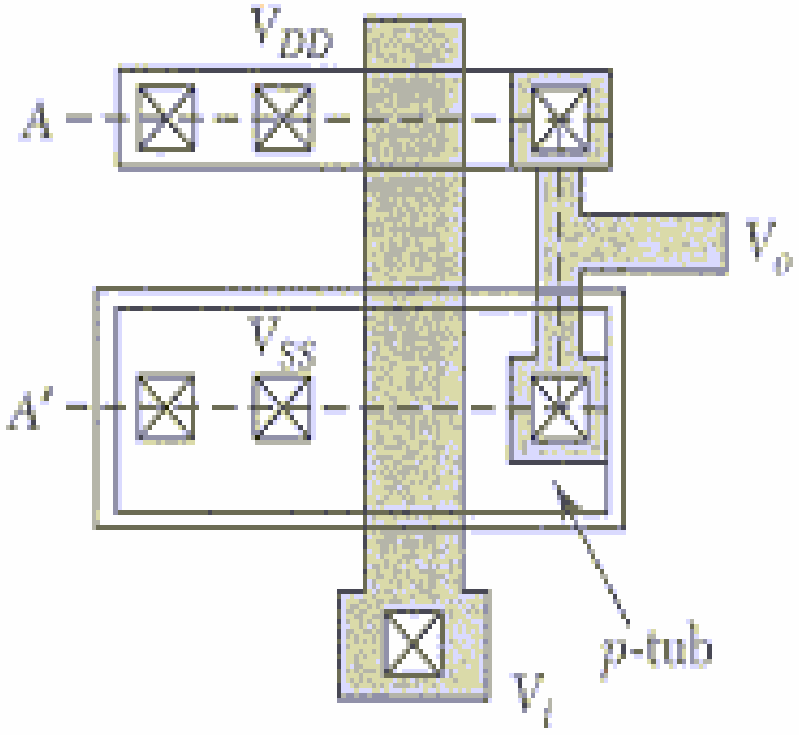


- p-well is implanted and driven into *n*-substrate (*p*-type dopant concentration must be high enough to overcompensate the *n*-substrate background doping).
- Subsequent processes for *n*-channel MOSFET in *p*-well are identical to nMOSFET.
- For *p*-channel MOSFET, B ions are implanted into *n*-substrate to form source and drain
- Because of *p*-well and steps needed for p-FET, the number of steps in CMOS fabrication is double that to make NMOS.

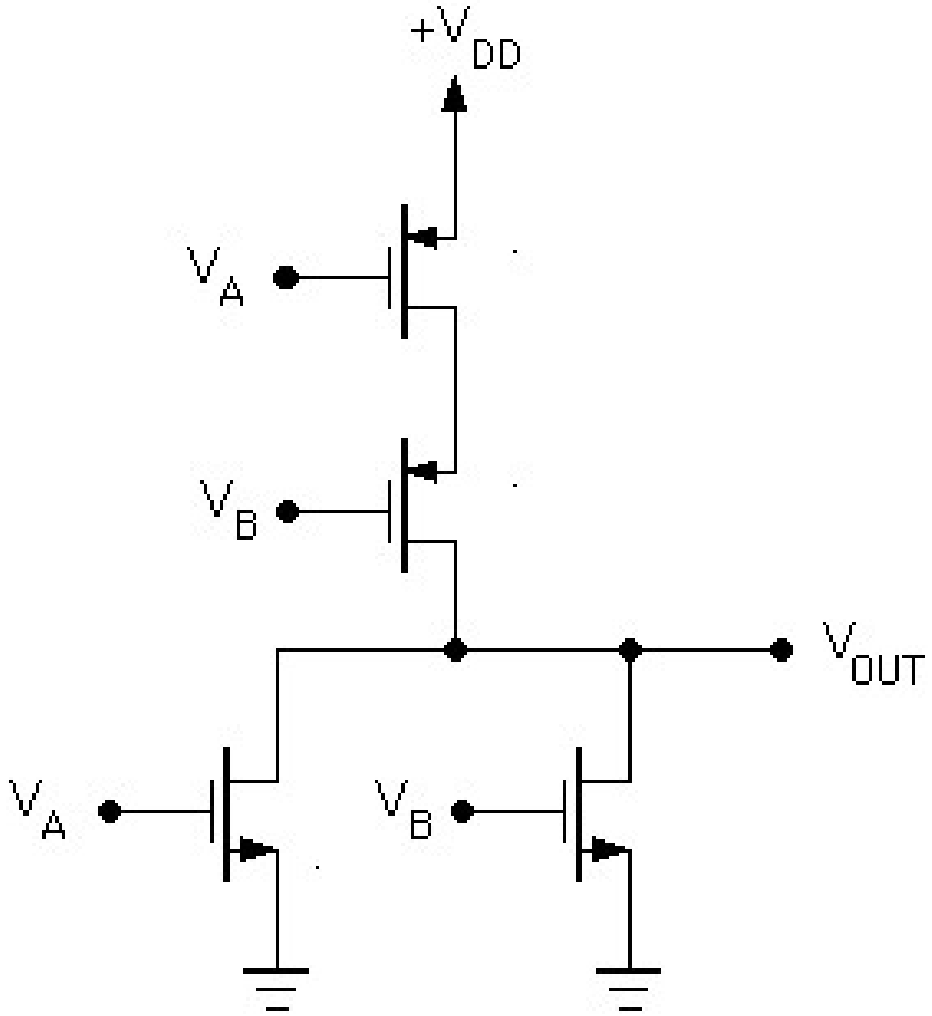
CMOS Inverter Layout



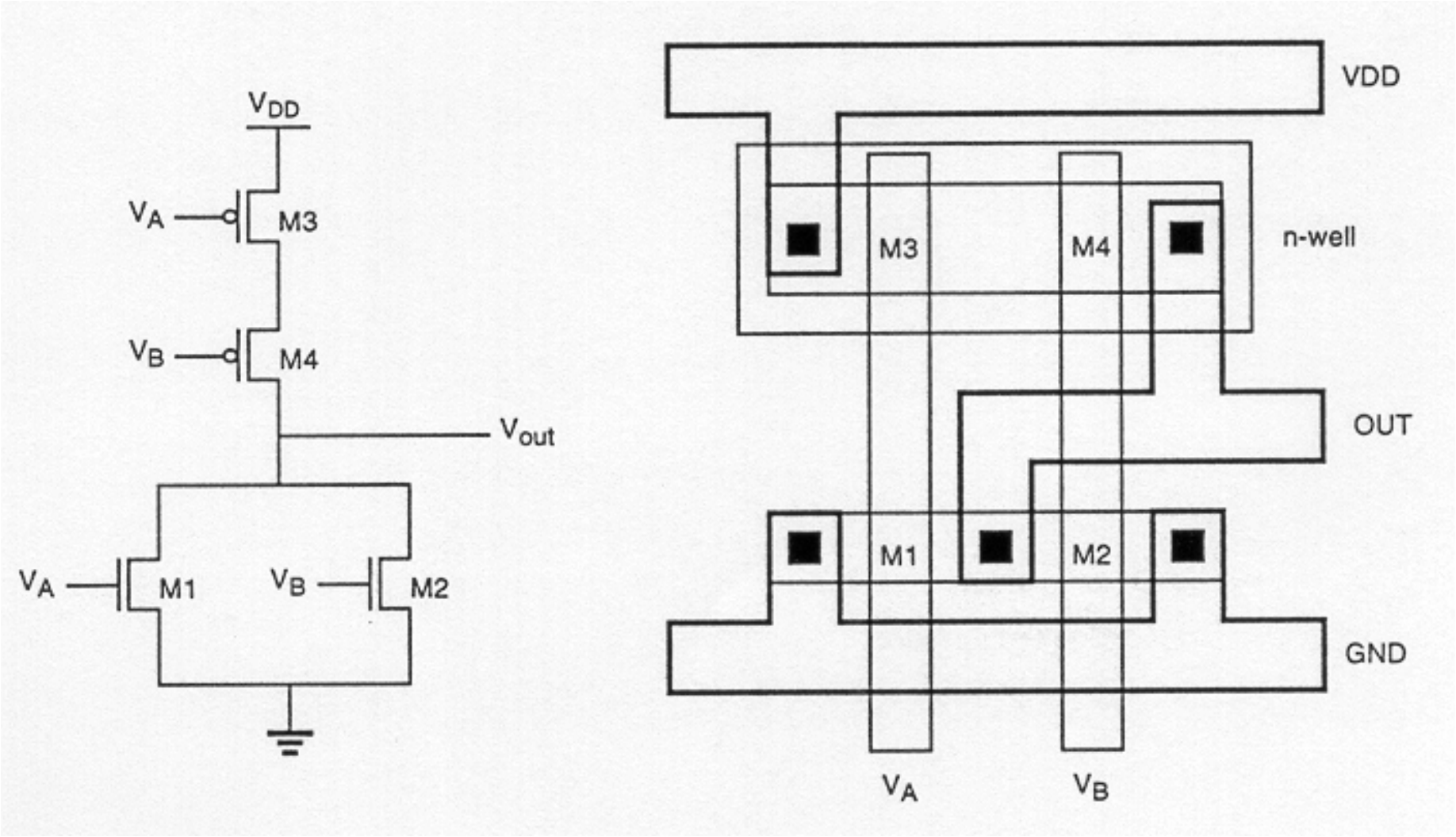




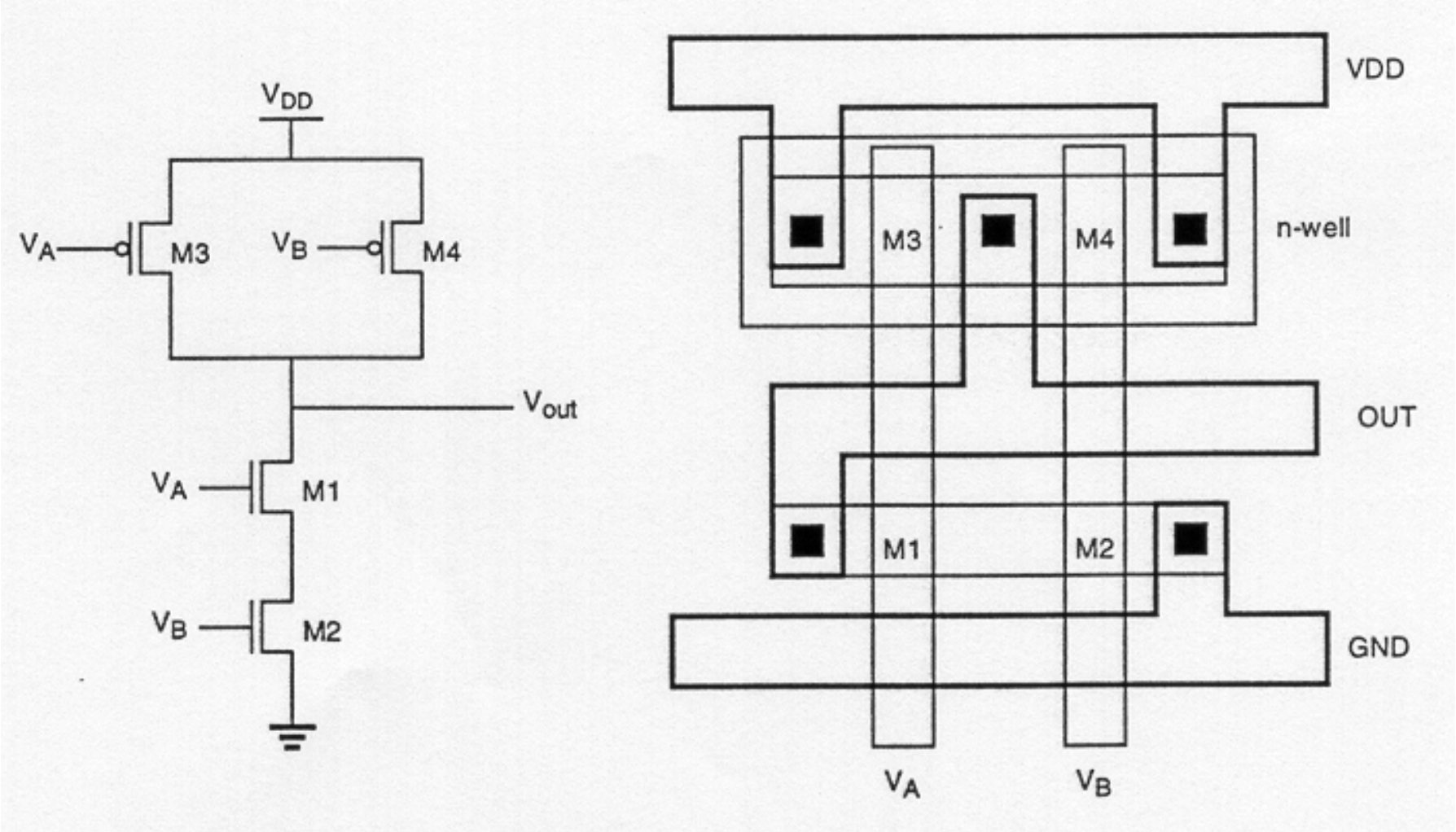
CMOS Logic Structures - NOR



NOR Layout



NAND Layout

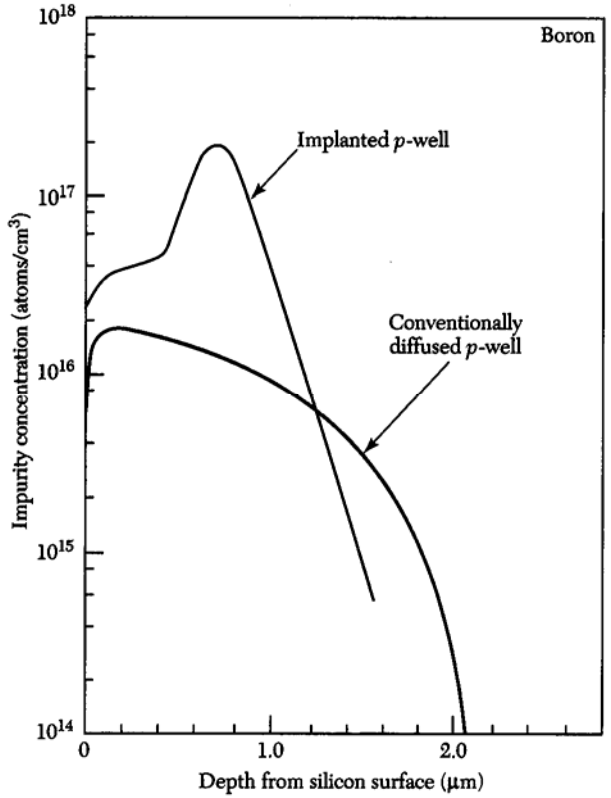


Well Types

- Single well – discussed previously
- Twin well
  - p-well and n-well side-by-side on lightly doped substrate
  - Disadvantage: needs high temperature processing (above 1050 ^{o}C) and a long diffusion time (>8 hours) to achieve the required well depth of 2 – 3 μm
- Retrograde
  - To reduce process temperature and time, high-energy implantation is used
  - The profile of the well in this case can have a peak at a certain depth in the silicon substrate.

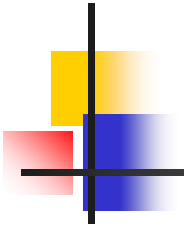
Retrograde Wells

- Advantages:
  - Reduced lateral diffusion and increase the device density.
  - Lower well resistivity
  - Chanstop can be formed at the same time as well implantation



Conventional Isolation

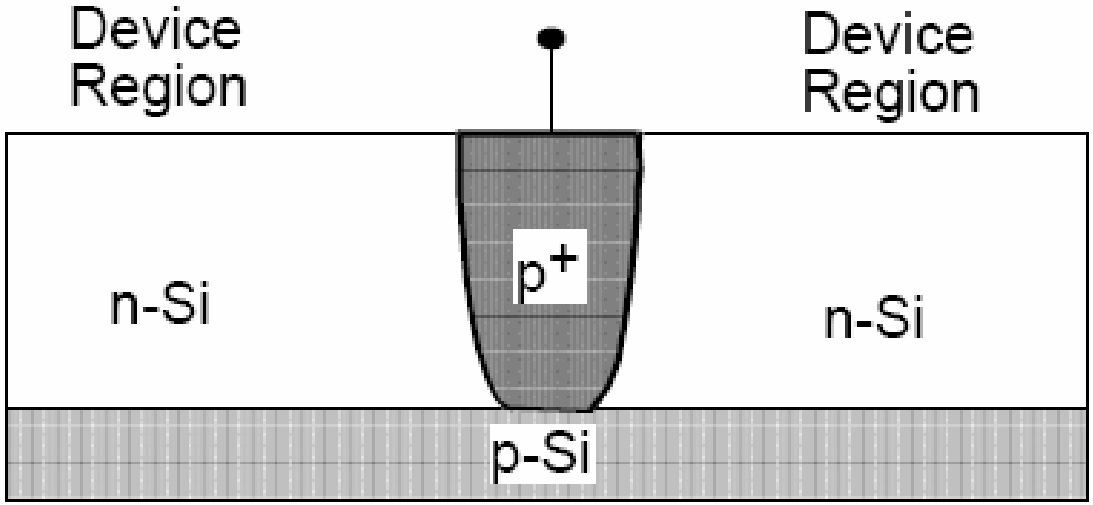
- Conventional MOS isolation process has disadvantages for deep-submicron (< 0.25 mm) fabrication:
  - High-temperature and long oxidation time result in encroachment of chanstop implantation to the active region, causing a threshold voltage shift.
  - Area of the active region is reduced because of lateral oxidation
  - Field oxide thickness is significantly less than that grown in wider spacings
- Trench isolation technology can avoid these problems.



Methods of Isolation

- pn Junction Isolation
- Oxide Isolation
  - Field Oxide Isolation
  - LOCOS (SILO, SWAMI etc)
- Trench Isolation
  - Shallow trench isolation
  - Deep Trench isolation
- Dielectric isolation
  - Silicon on Insulator

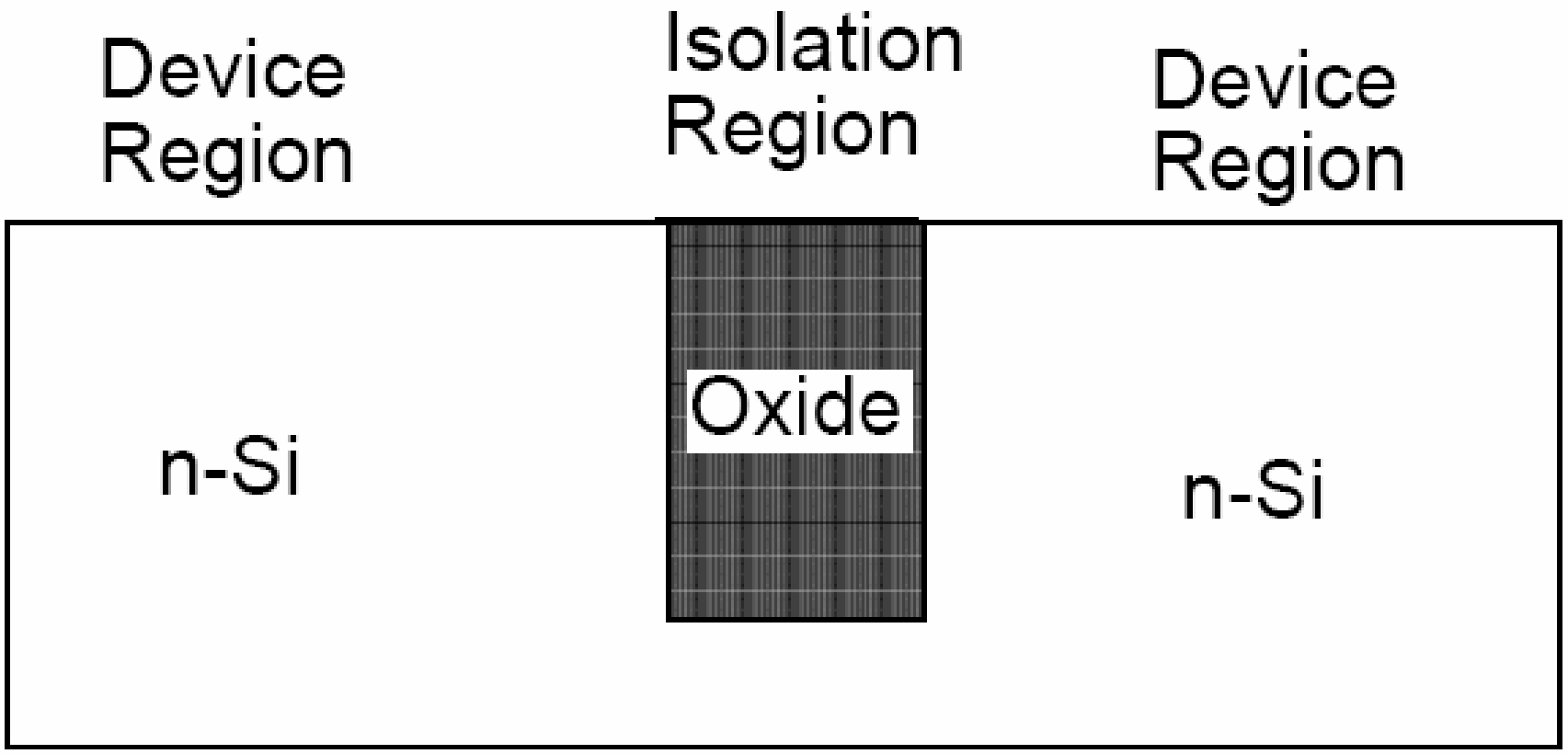
Reverse Biased Junction Isolation



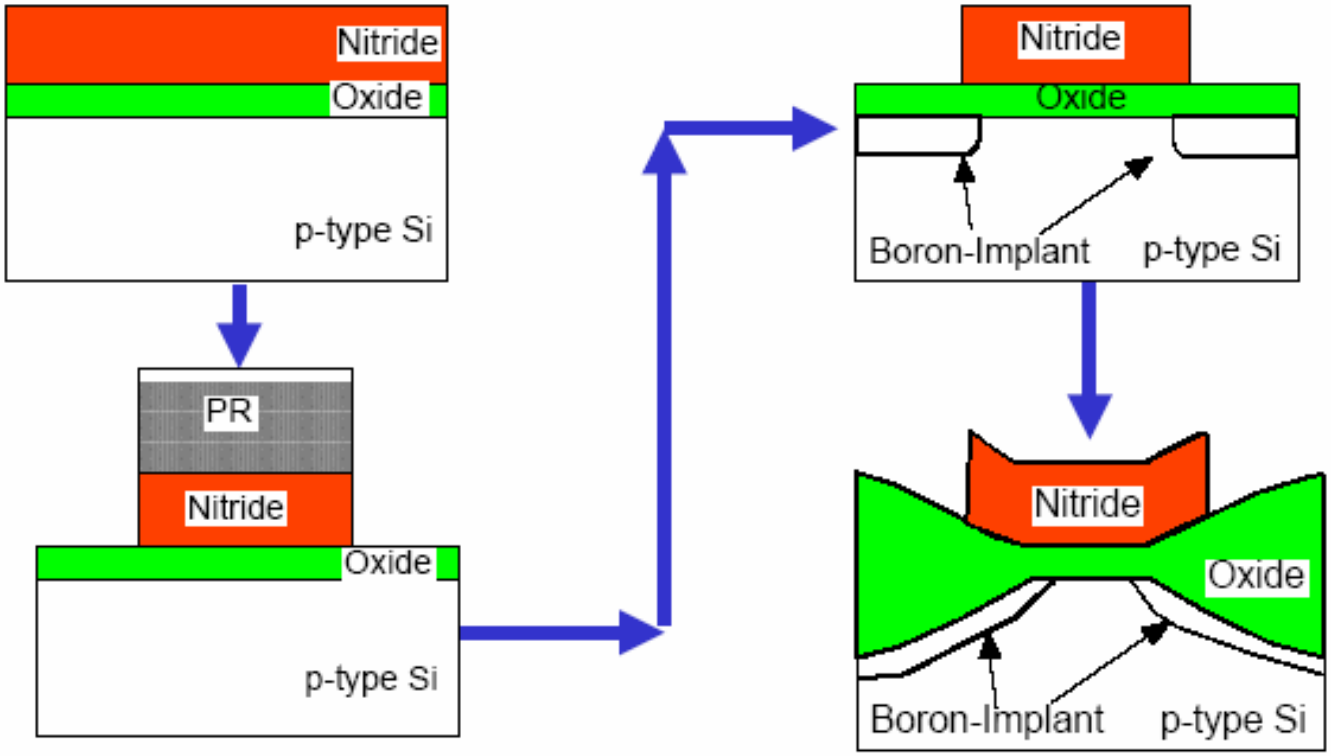
Issues

- Parasitic MOSFET threshold voltage
  - Cannot withstand high signal voltages
- Parasitic Capacitance
  - Slows down circuit speed
- Low Density
  - Increased chip area and lower speed

Recessed Oxide Isolation



Local Oxidation of Silicon (LOCOS)

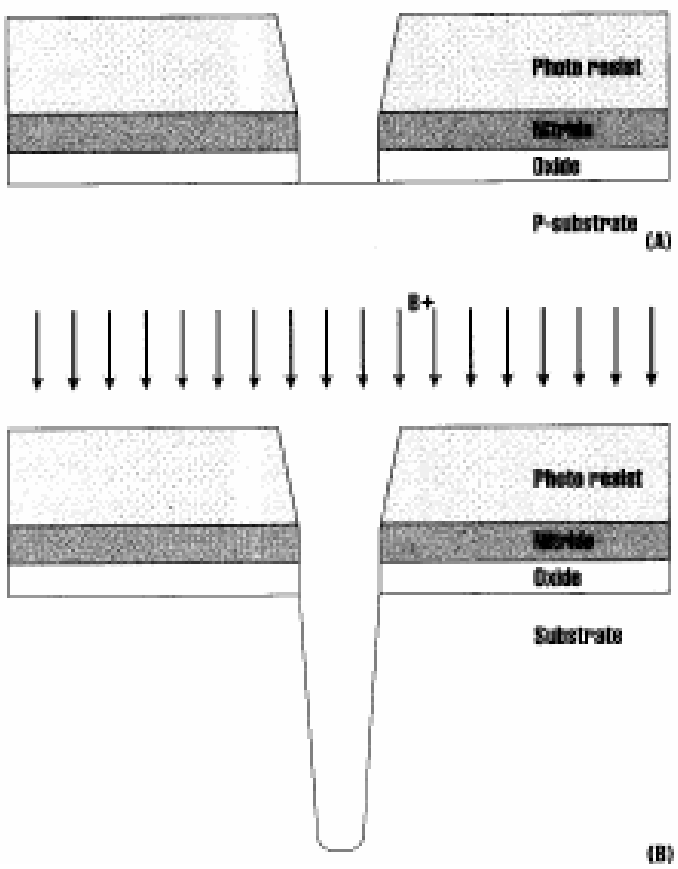


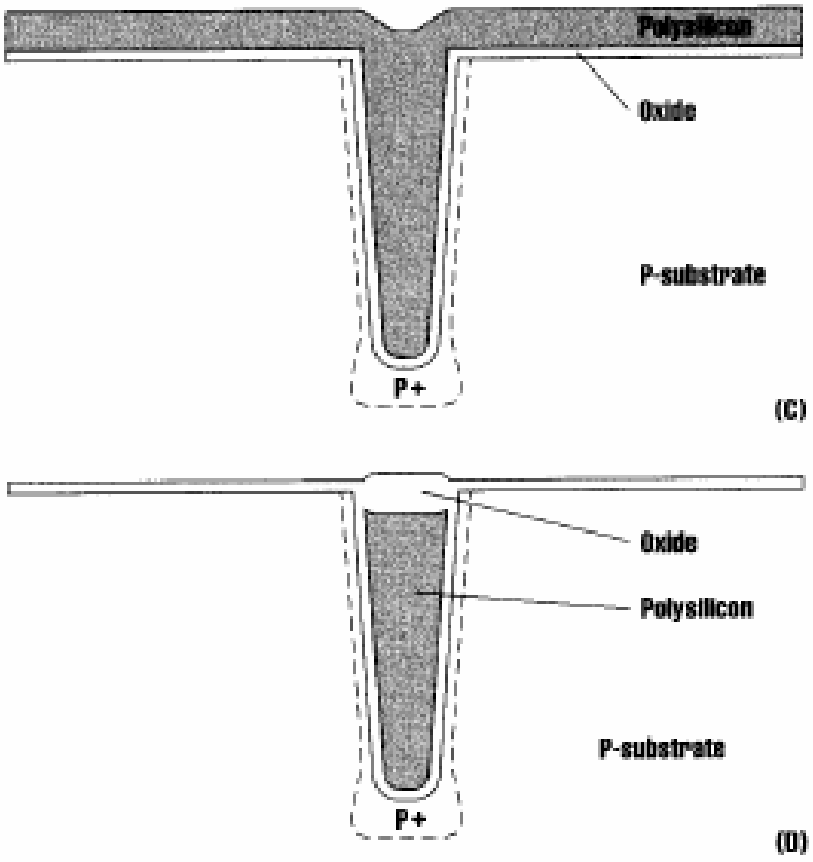
- Oxidant(s) **cannot** diffuse through the nitride to the Si/SiO_2 interface, hence there is no oxidation under nitride (device region)
- Initial thin oxide layer used for reducing stress
- Some of the nitride is oxidized during LOCOS
- Nitride stripped using hot phosphoric acid

LOCOS Issues

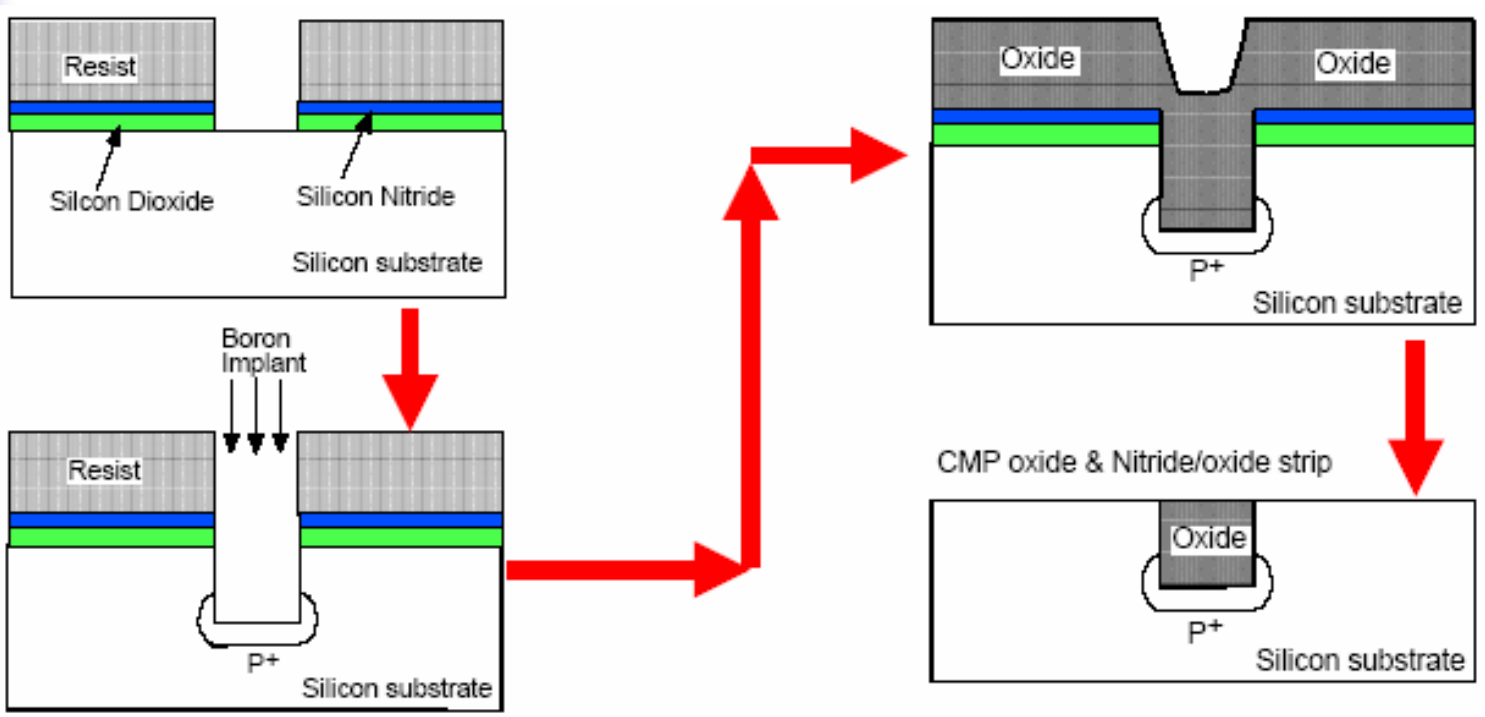
- Birds beak formation limits circuit density
- Implant required to shift field oxide threshold
- Topology/Planarity issues for Lithography
- Stress and dislocation generation
- Lateral encroachment of dopant leading to narrow channel effect because of diffusion
- New variations of LOCOS solve these problems

Deep Trench Isolation



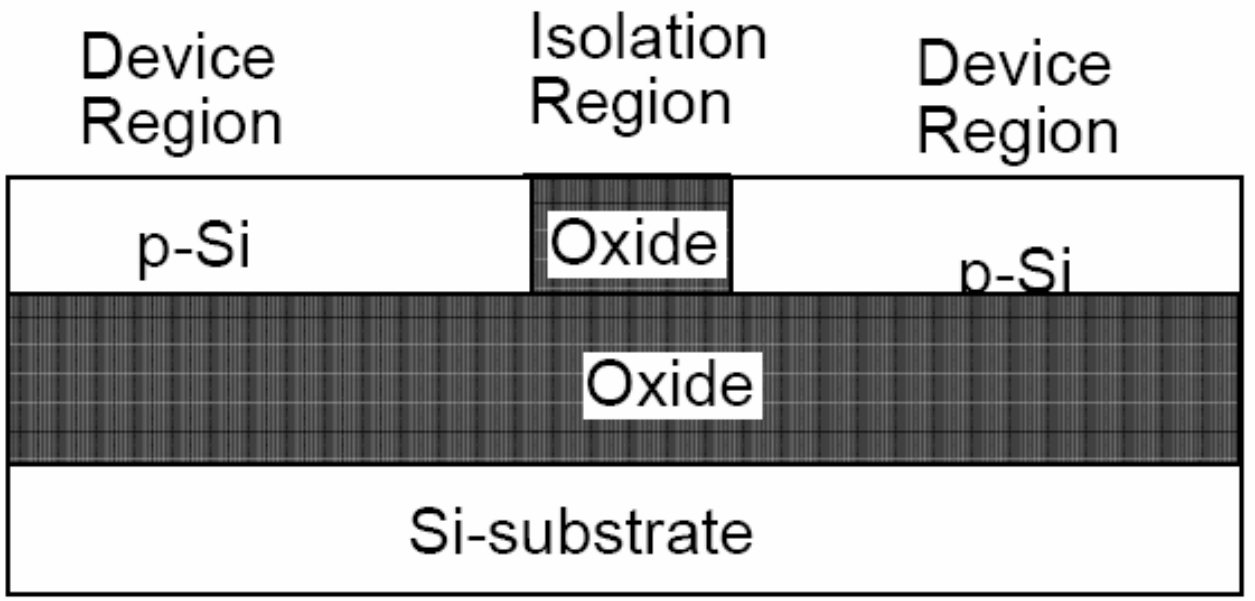


Shallow Trench Isolation

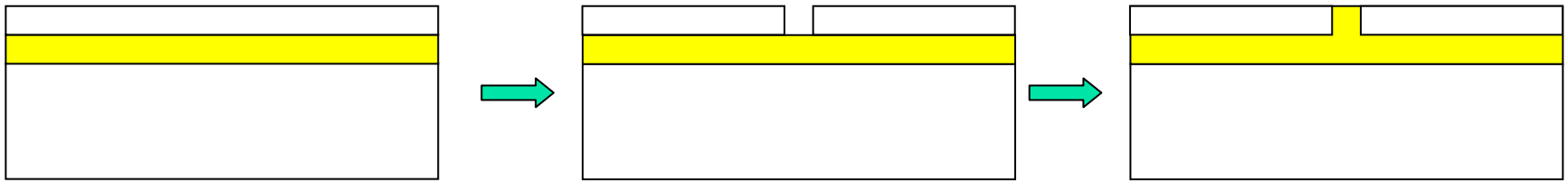


- Growth of pad silicon dioxide and deposition of silicon nitride as in LOCOS
- Implant trench to increase field threshold and growth of liner oxide for passivation and smoothing
- Trench fill with deposited oxide (high density plasma oxide)
- CMP for planarization
- Oxide densification
- Nitride strip in hot H_3PO_4

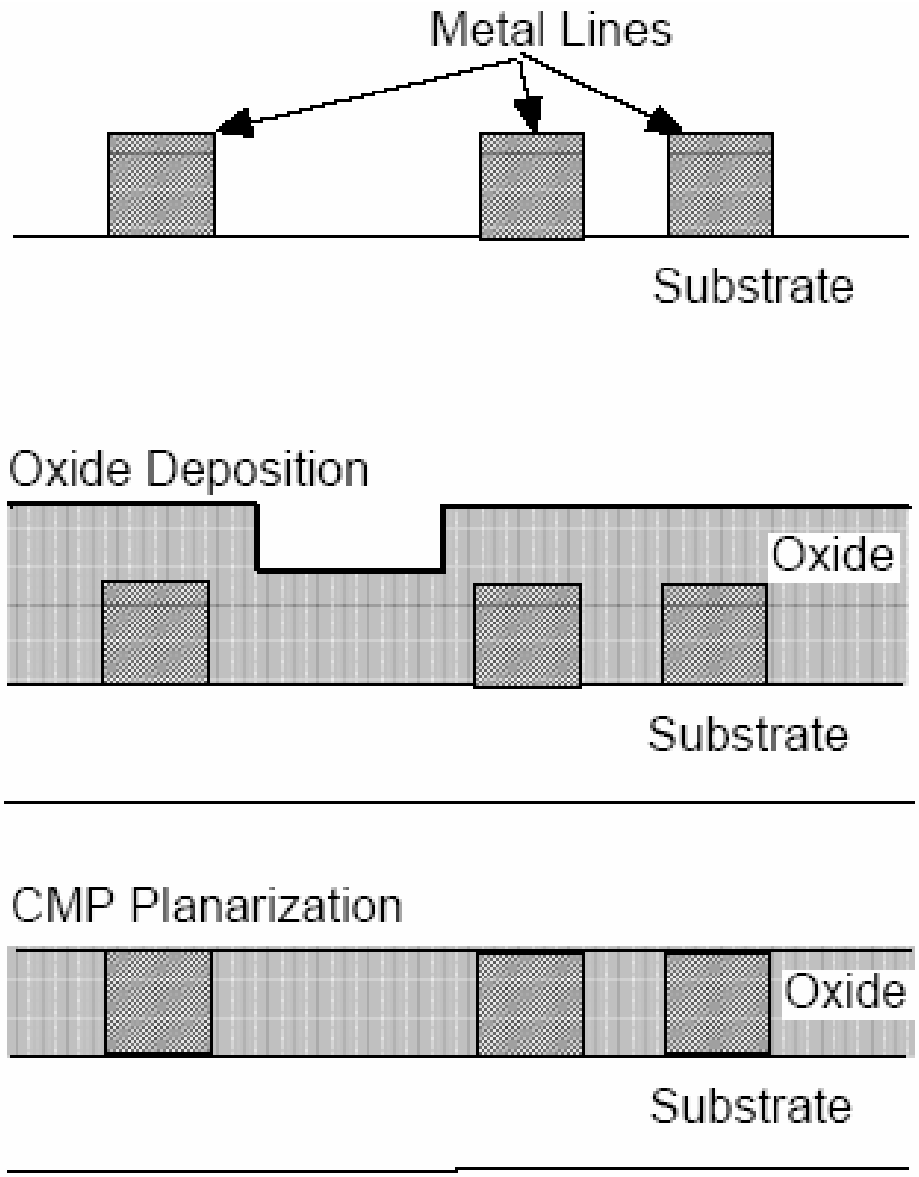
Silicon on Insulator (SOI)



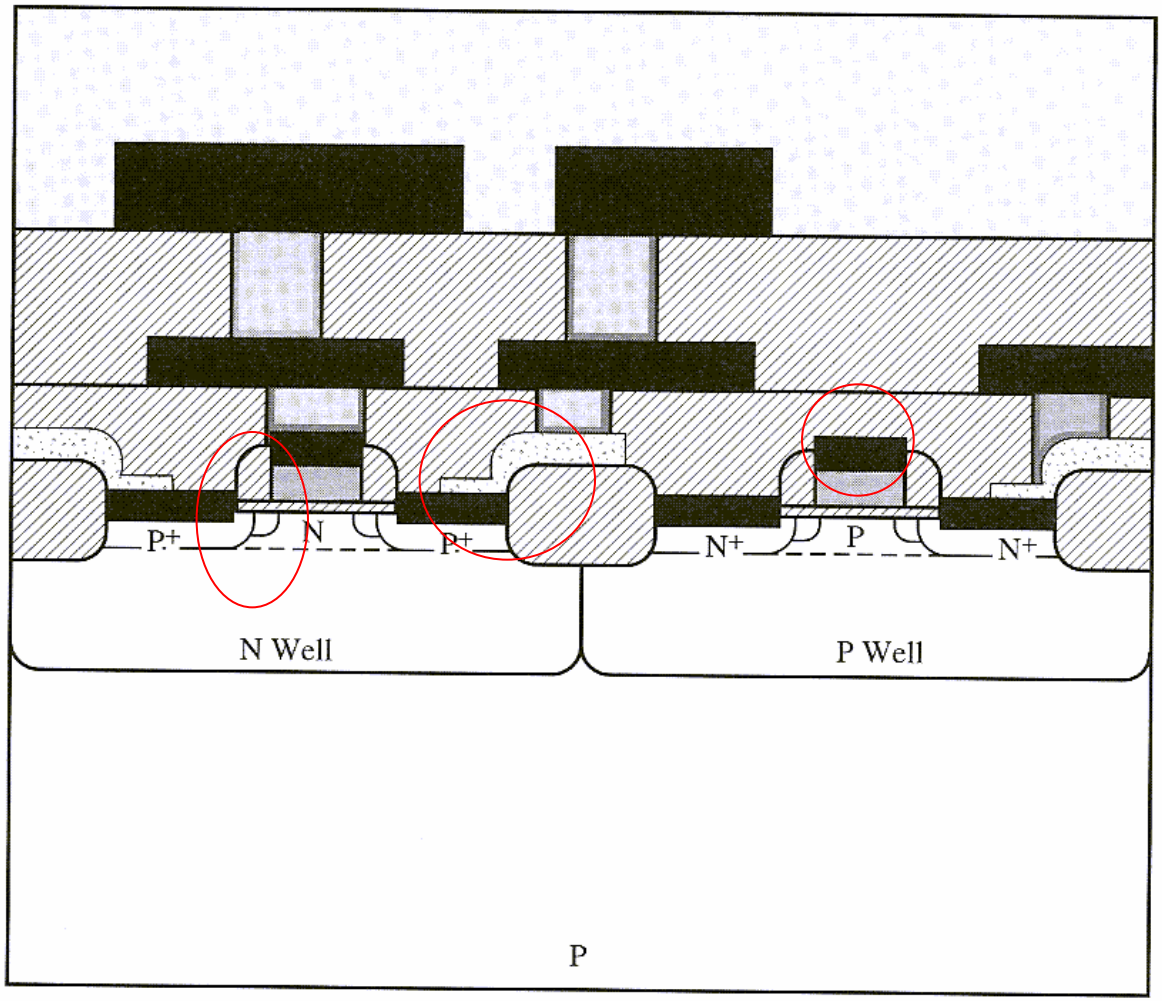
- Start with a SOI Wafer



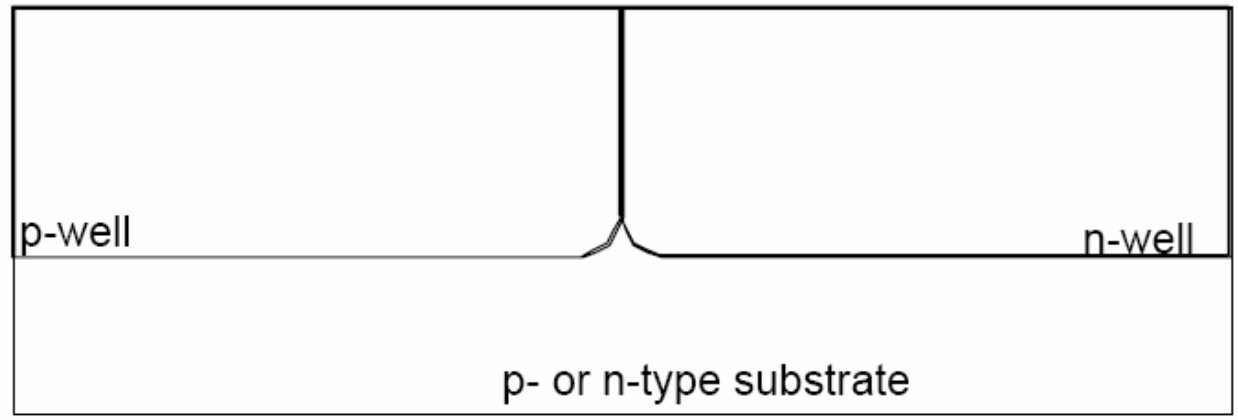
Interconnect Processes

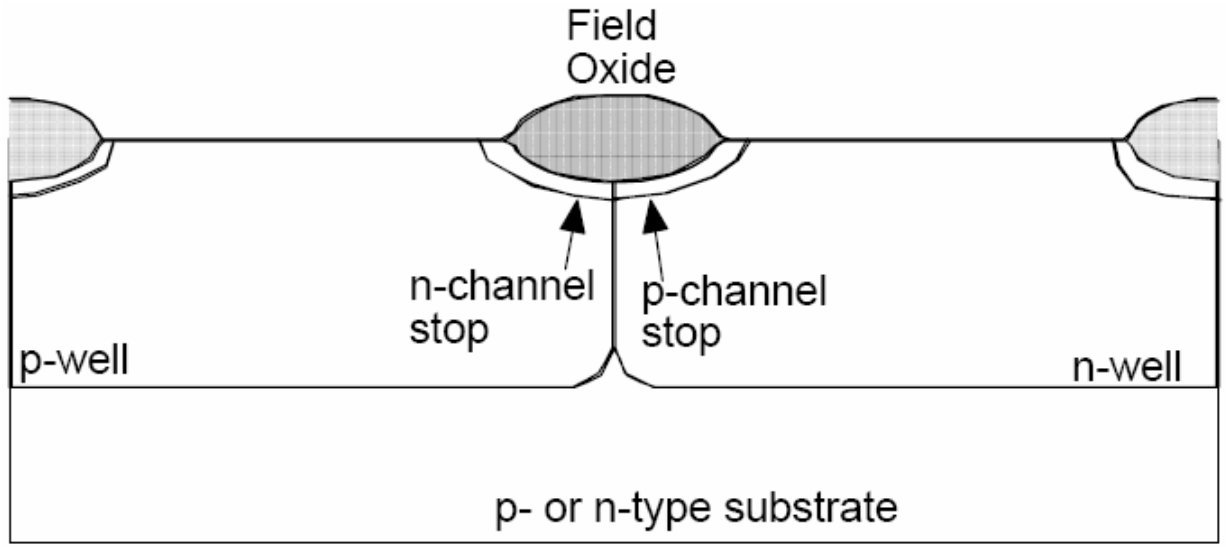


Current CMOS Process



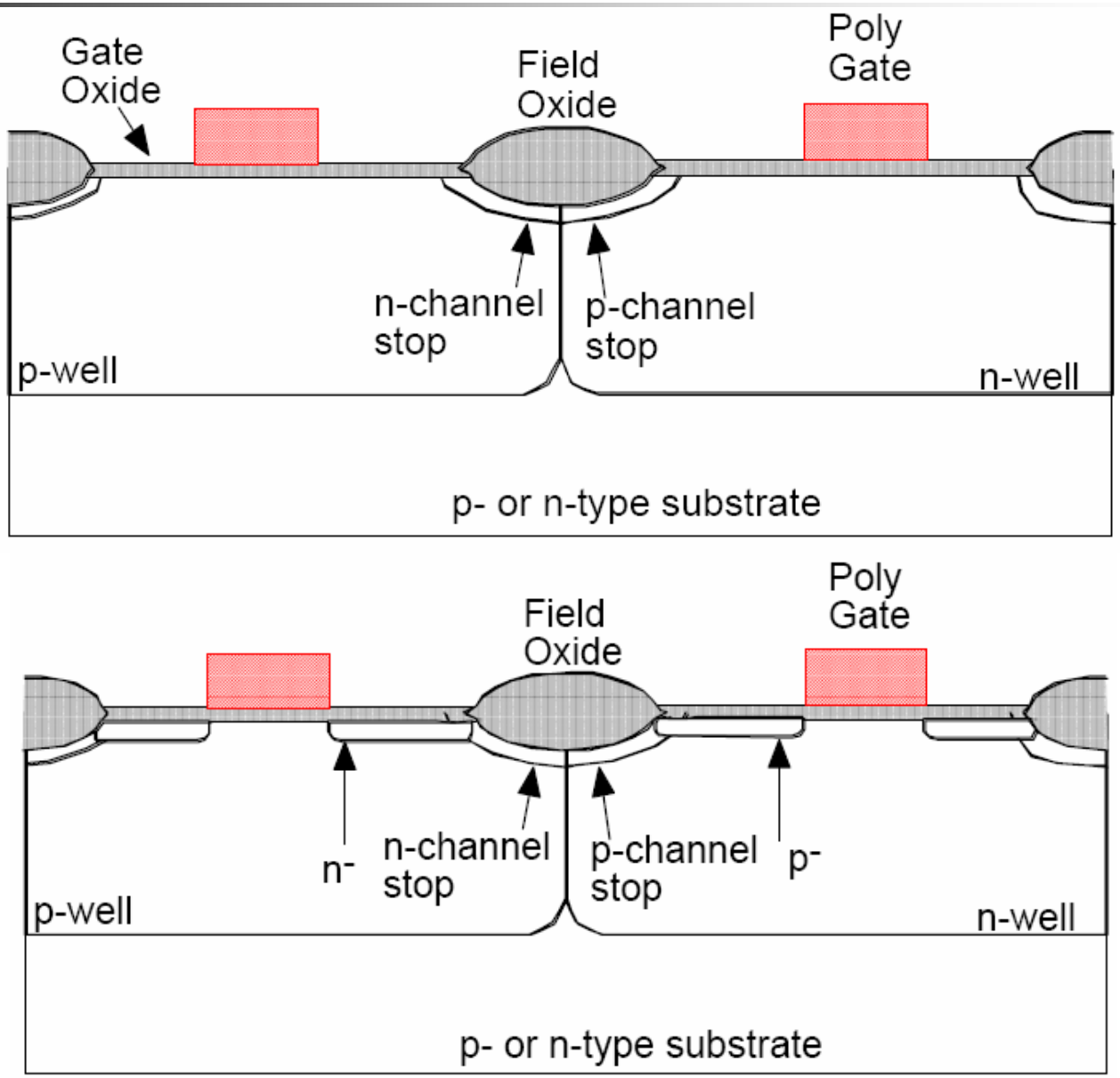
Well Formation and Isolation



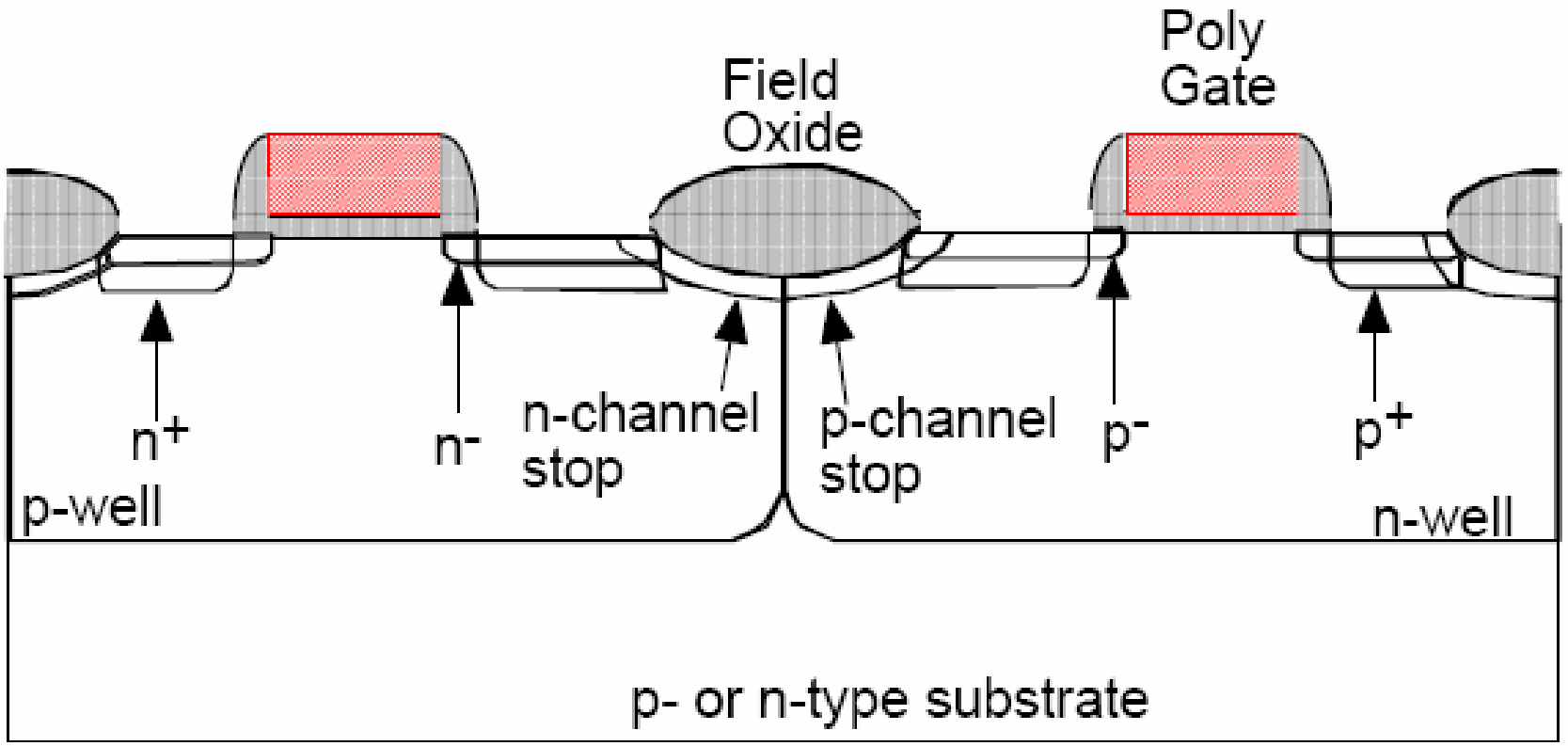


- Two masking steps for implant of n and p well
- Combined anneal (if possible)
- Two masks for 'channel-stop' implants
  - Self-aligned to LOCOS

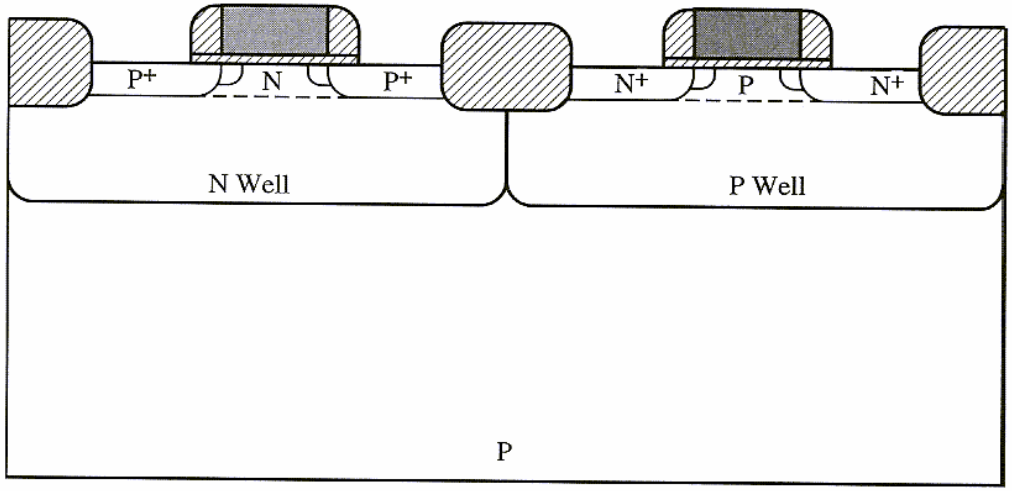
Poly Gate and Light-Doped Drain



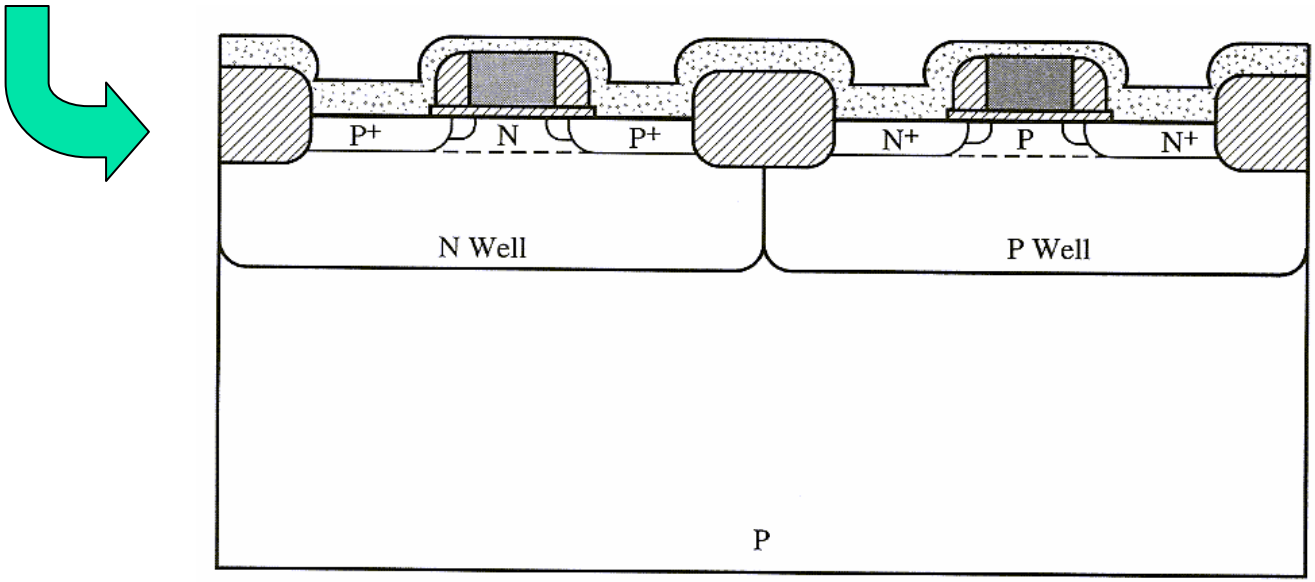
Sidewall Spacer and S/D Implant



Silicide Process

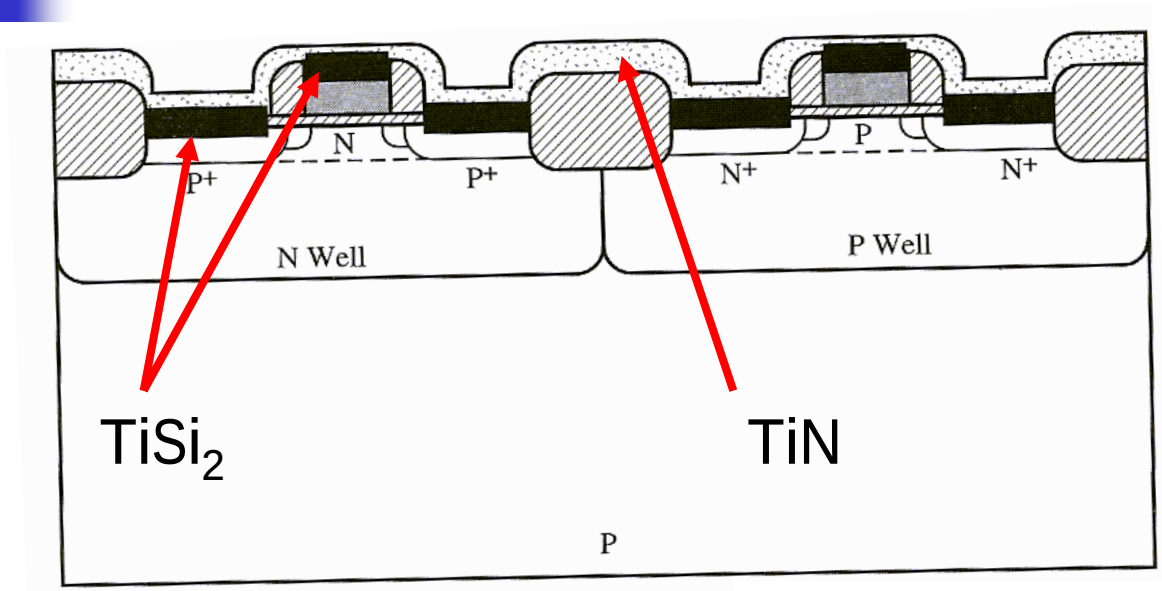


Deposit Ti



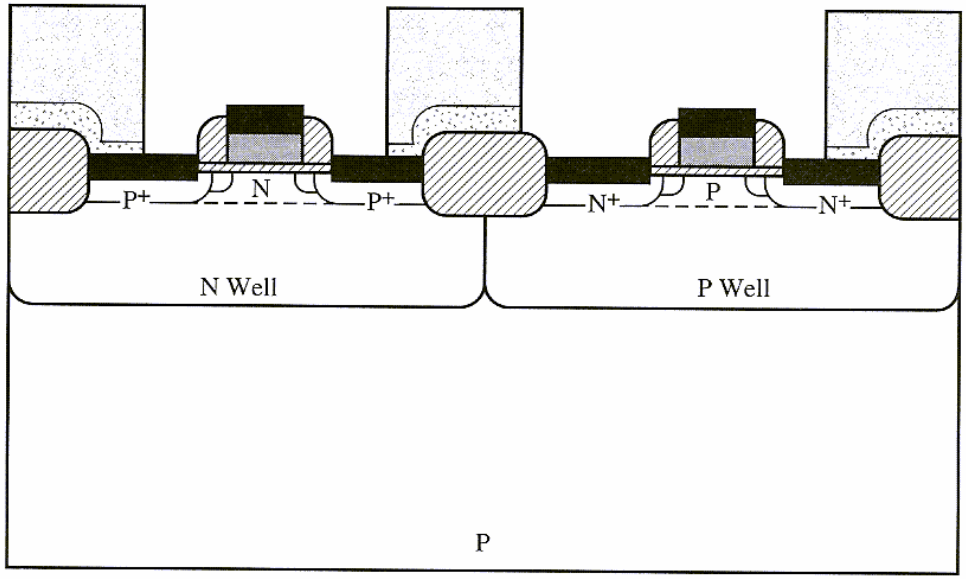
Silicide Formation

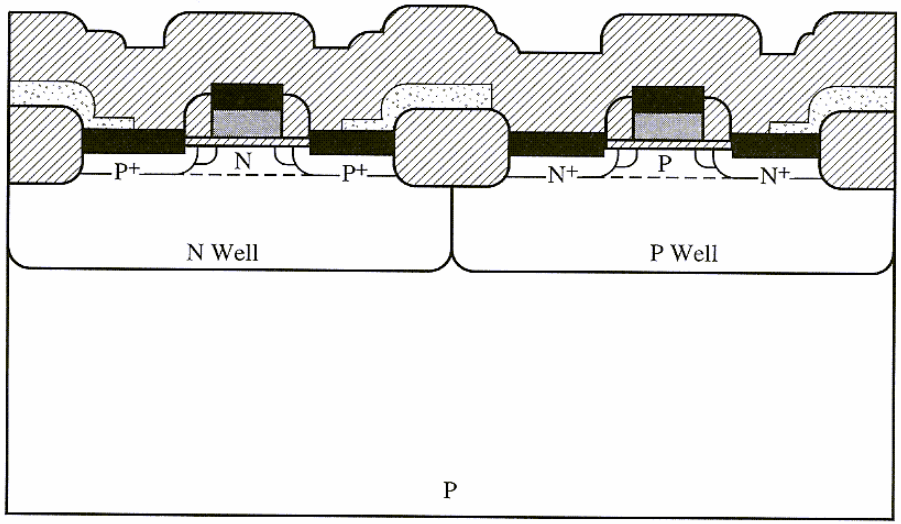
Silicide	Resistivity (μΩ-cm)	Anneal Temperature (°C)	n-type Barrier (eV)
$TiSi_2$	13-16	900	0.6
$TaSi_2$	35-45	1000	0.59
$MoSi_2$	90-100	1100	0.55
WSi_2	70	1000	0.65
$CoSi_2$	16-20	900	0.65
PtSi	28-35	600-800	0.86



Anneal in N_2

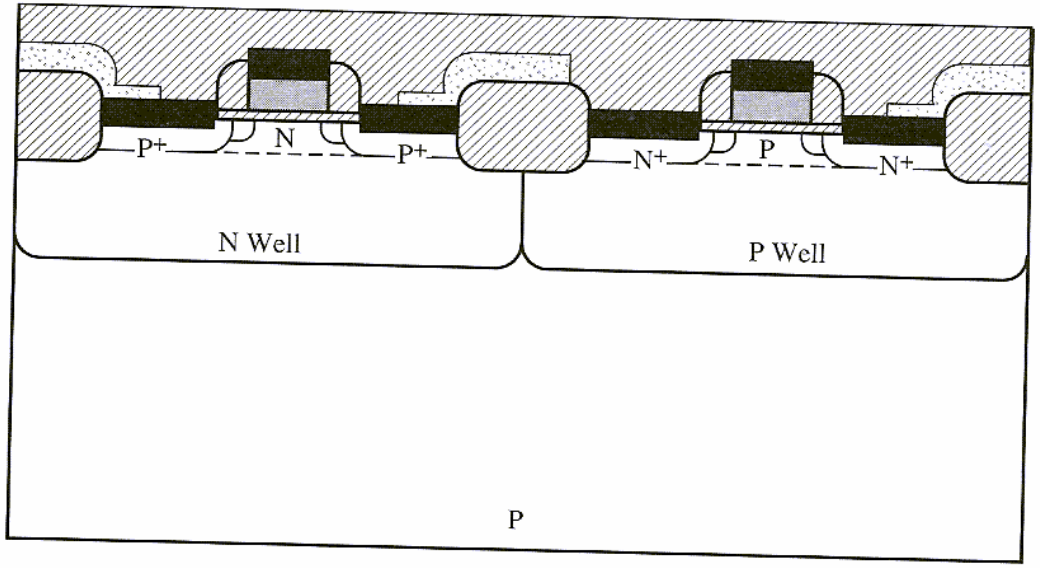
Photo and
etch TiN (defines
local interconnect)





Deposit insulator (oxide)

Planarize



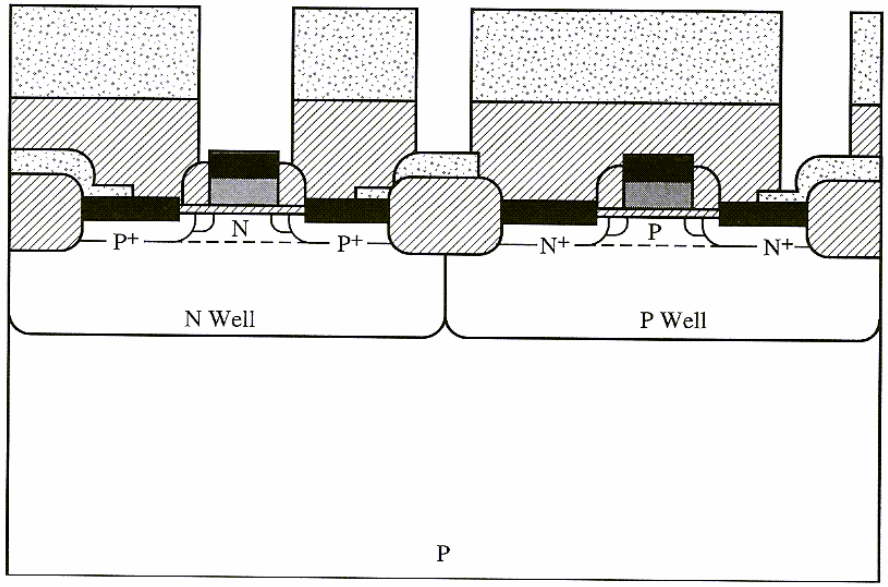
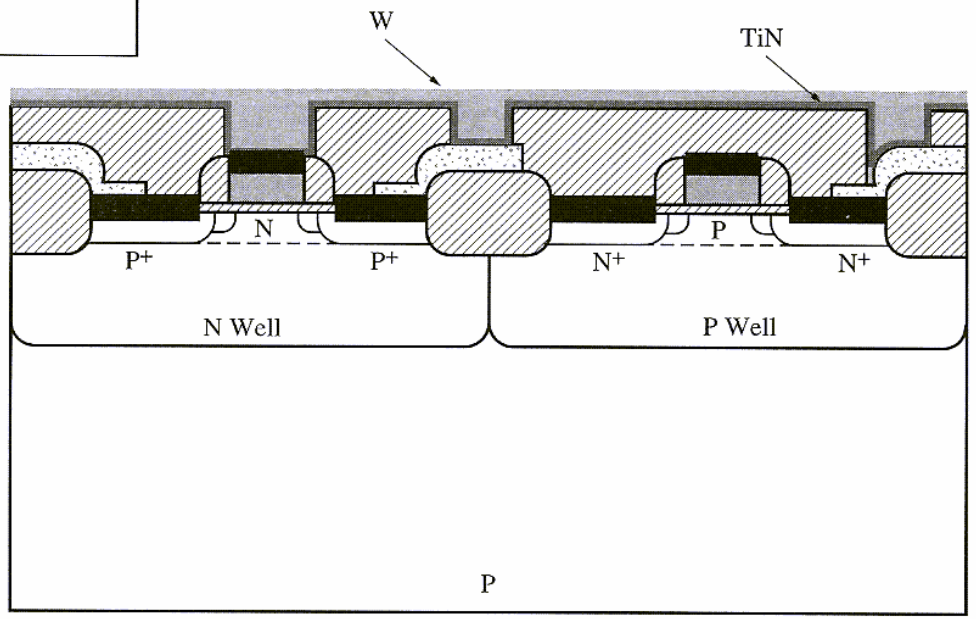
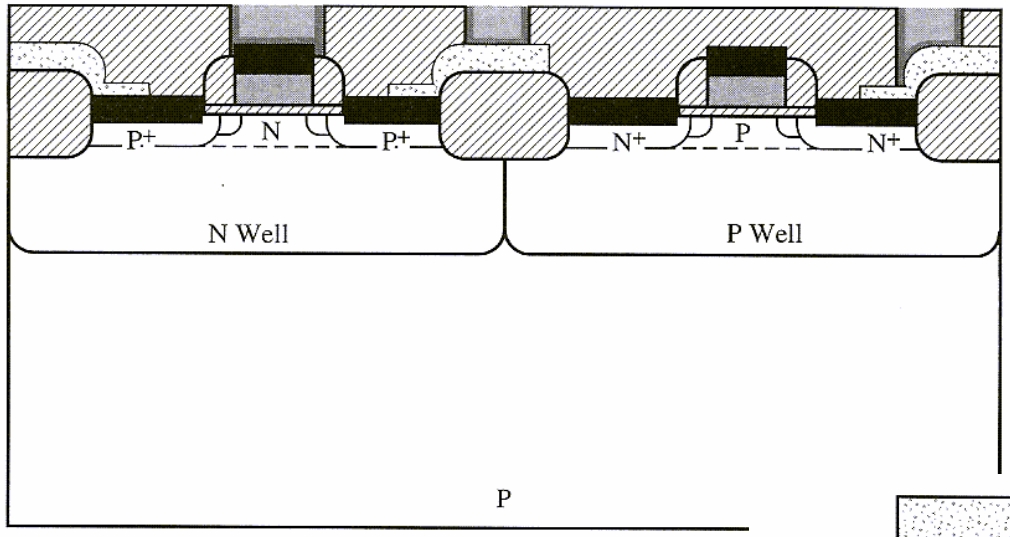


Photo and
etch oxide

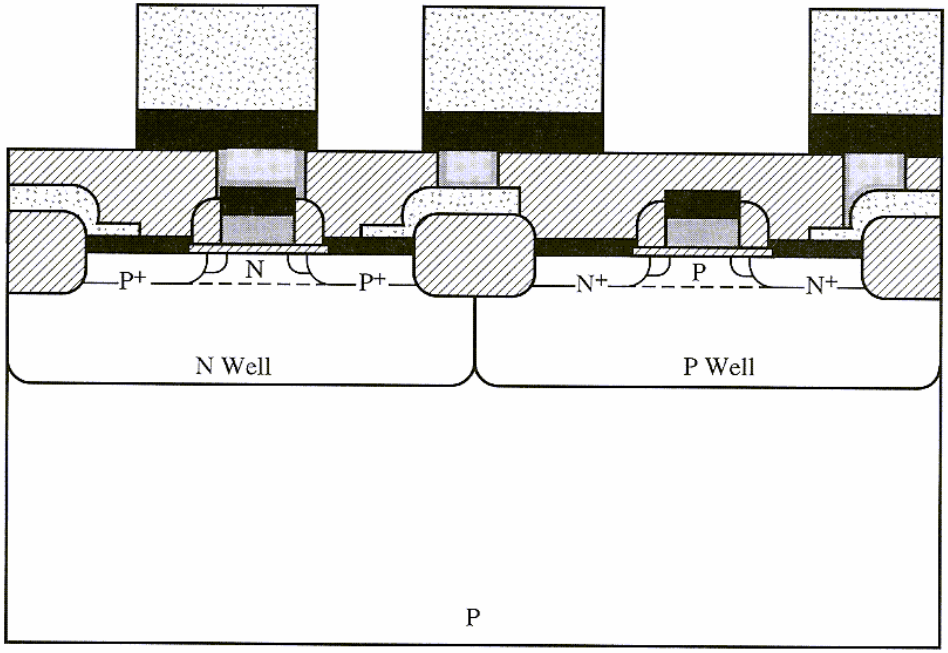
Deposit liner (TiN),
plug metal (W)



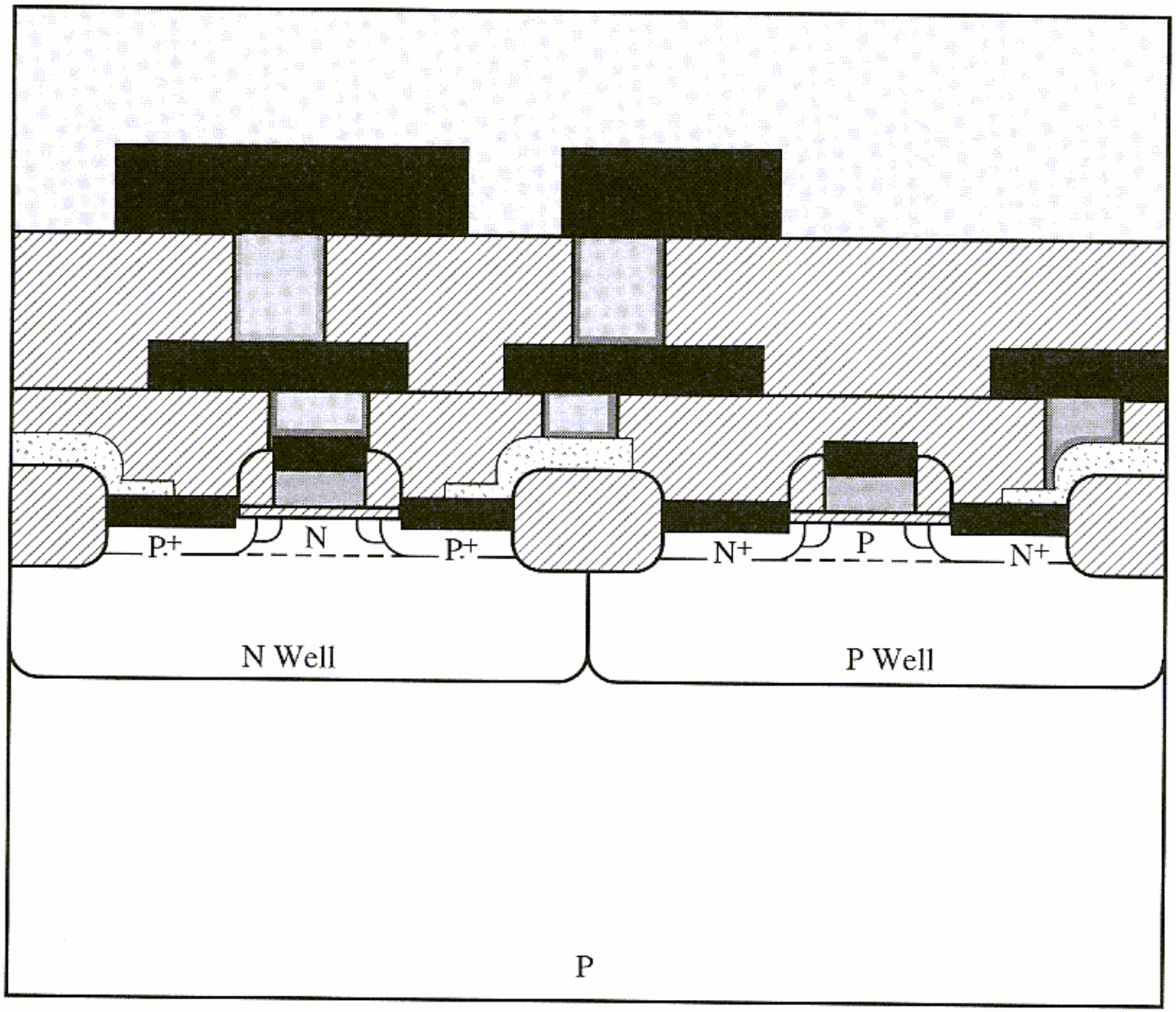


Planarize

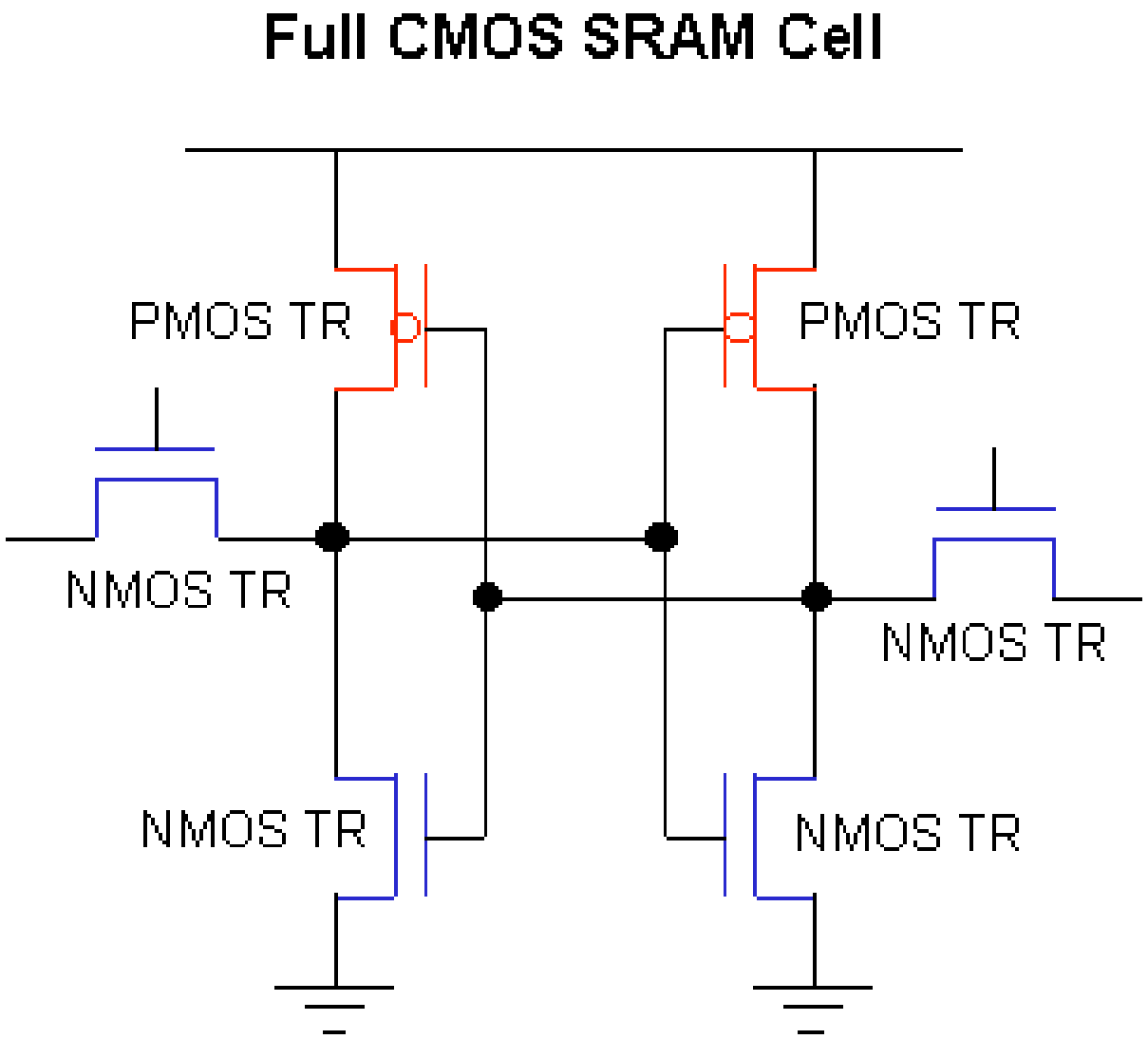
Deposit and pattern Al



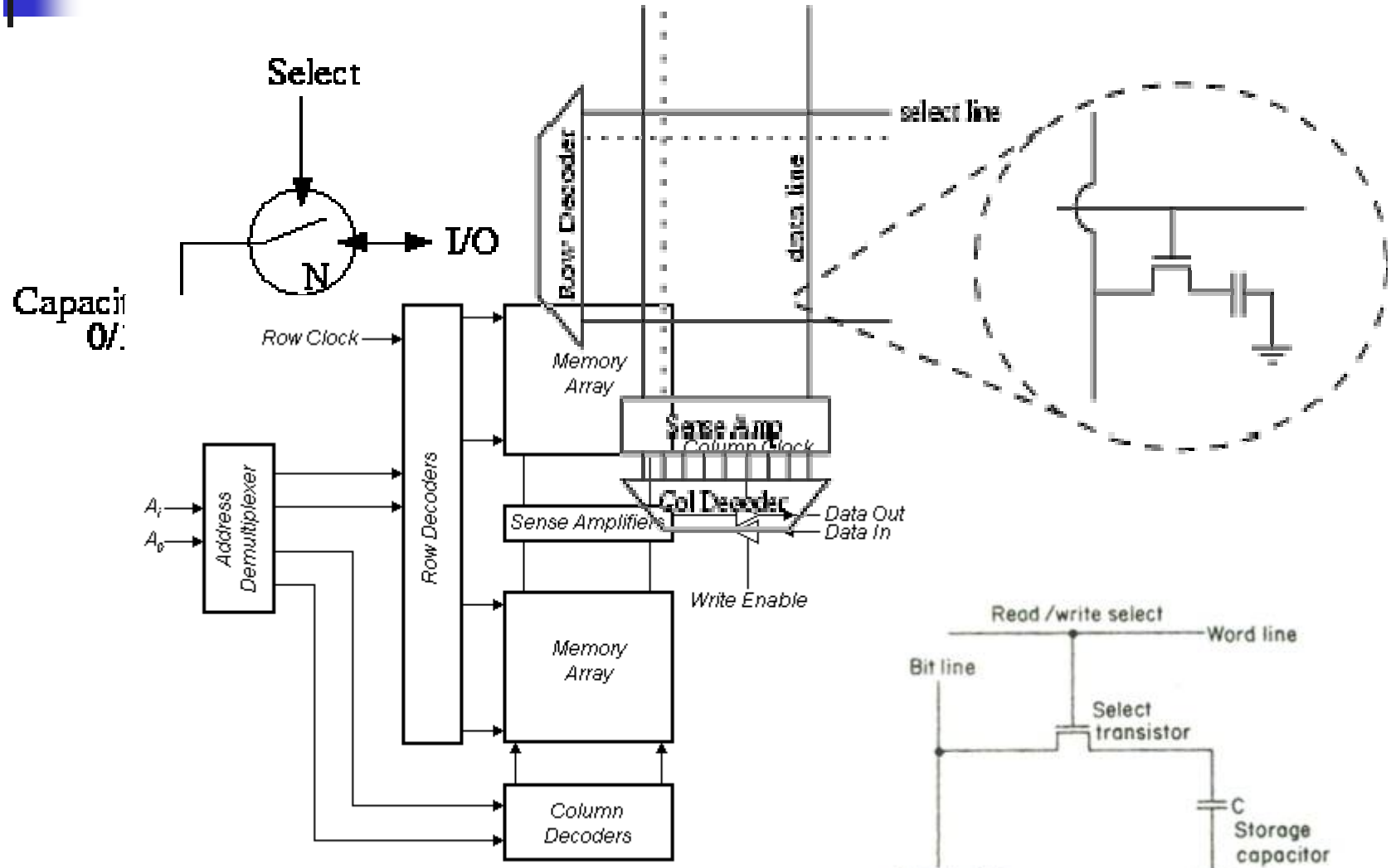
Final Structure



CMOS SRAM (6T Cell)



Single Transistor DRAM



Internal Architecture of a DRAM