Intel's EUV Lithography Process Line

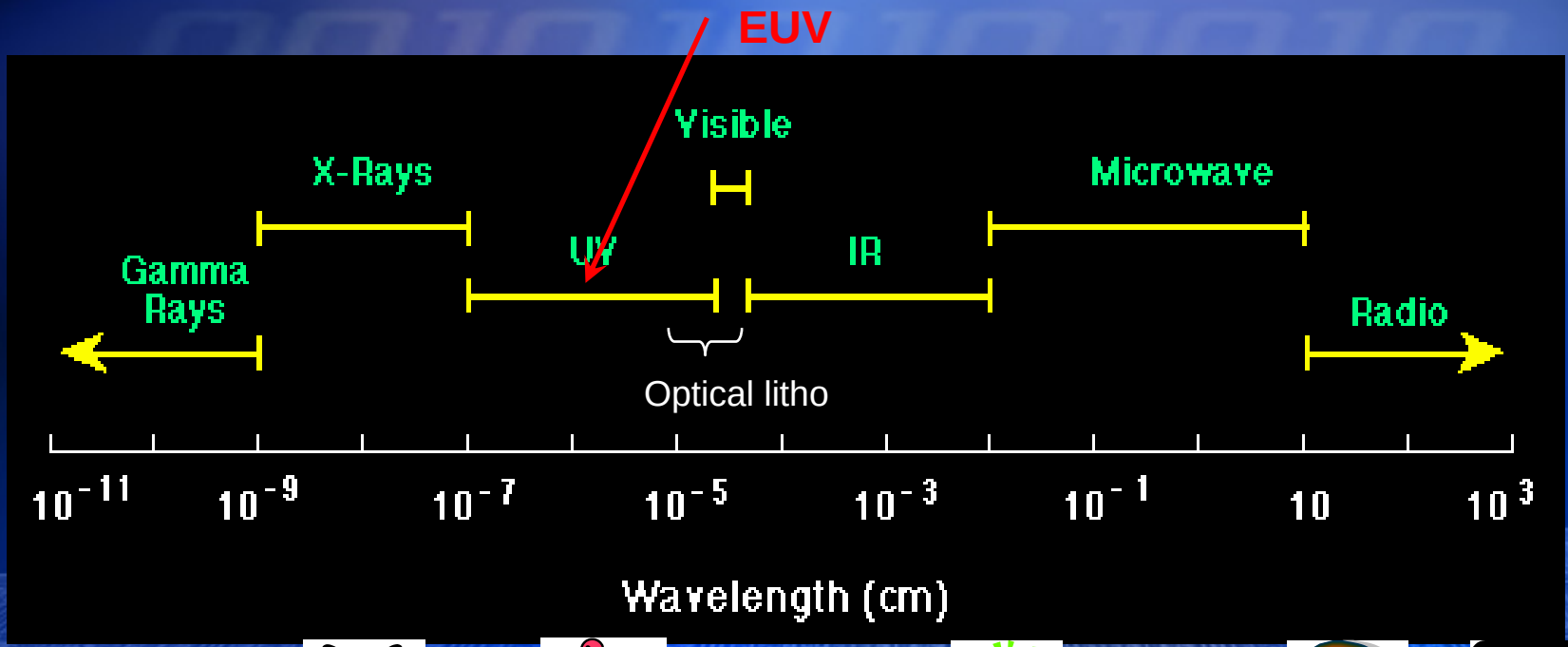
Ken David
Director, Components Research
July 2004

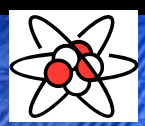
What are we announcing?

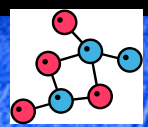
- Intel reached an important milestone as it progresses toward the deployment of EUV lithography, targeted for 2009 production, with the installation of the world's first commercial EUV lithography tool, called a Micro Exposure Tool (MET).
- The MET is part of the world's first integrated EUV lithography process line and is linked with an automated track that includes resist coating and developing operations (as opposed to stand-alone tools), indicating that this technology is moving out of the research lab toward a pilot line environment.
- Intel plans to develop its EUV masks in-house, and to that end has successfully established an EUV mask pilot line, including the world's first commercial EUV mask making tools, an e-beam mask repair tool and a mask blank defect inspection tool.
- Intel is actively working with the industry on the timely development of EUV lithography through R&D, strategic investments and joint development programs with EUV lithography companies such as Media Lario, Cymer, and NaWoTec.
- The results announced today show that Intel is positioned to be the first company to deploy EUV lithography, further extending Moore's Law into the next decade.

What is EUV Lithography

- **Uses light with a very small wavelength (13.5 nm, or 1.3×10^{-6} cm) -from the Extreme Ultra Violet region of the light spectrum - to transfer images from a mask onto a silicon wafer**




atom


molecule

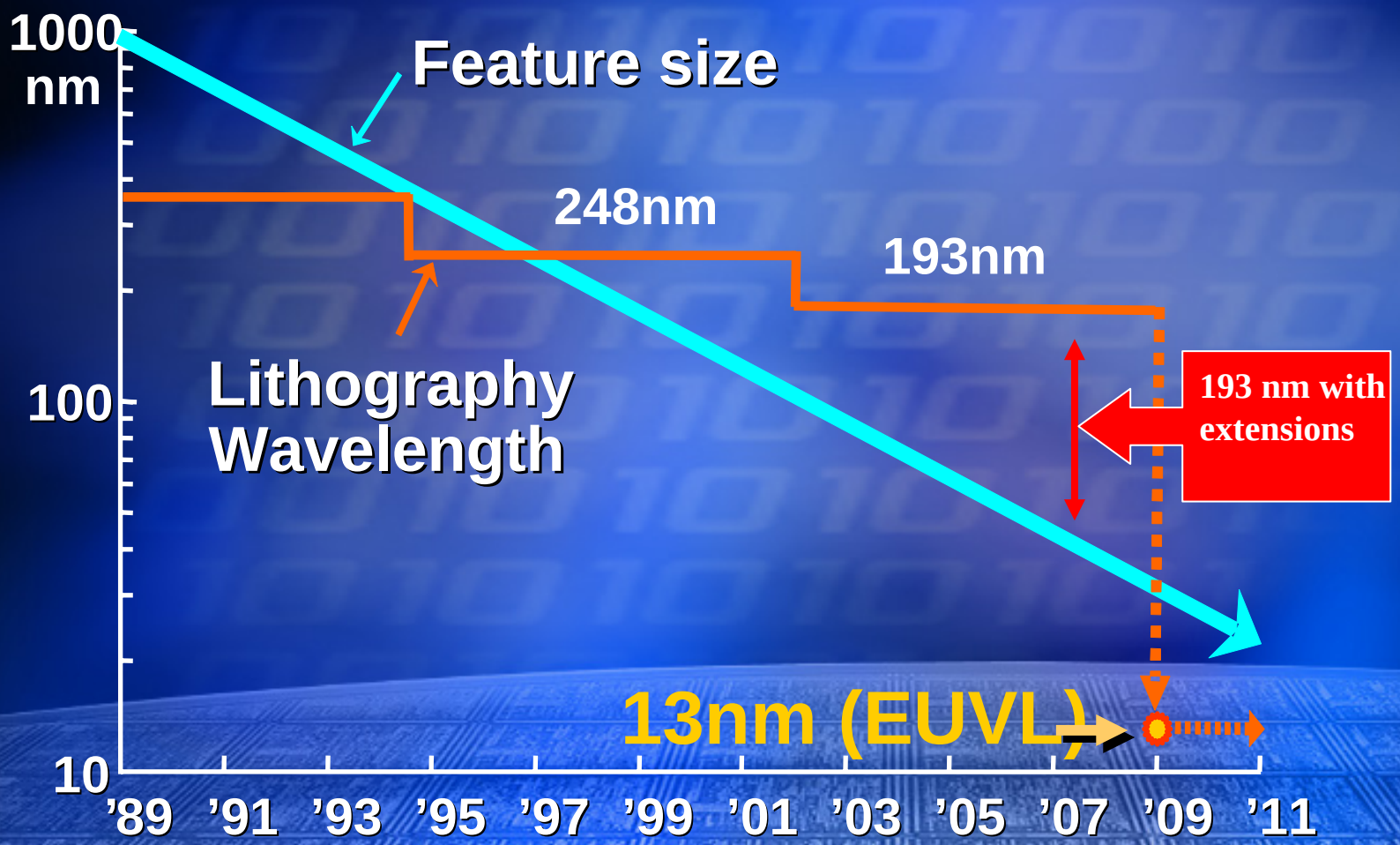

thickness of a dollar bill


softball


house

Lithography Challenge

Feature size scaling faster than wavelength reduction

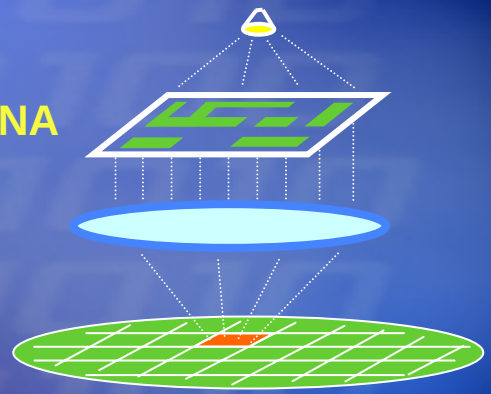


PSM used extensively in today's technology

EUV is an extension of optical Lithography

Similarities

- Resolution and Depth of focus scale with NA and wavelength **Minimum Feature Size = k1 λ / NA**
- Uses reduction optics
- Builds on optical lithography experience base
- Supports optical extension tricks – off axis illumination, phase shift masks, OPC
- Employs step and scan printing

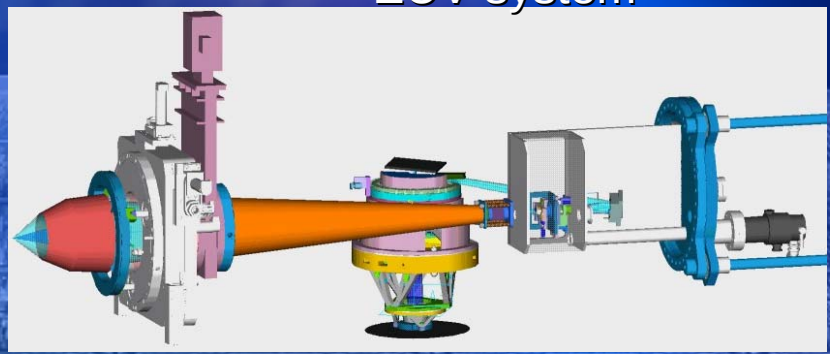


Optical system

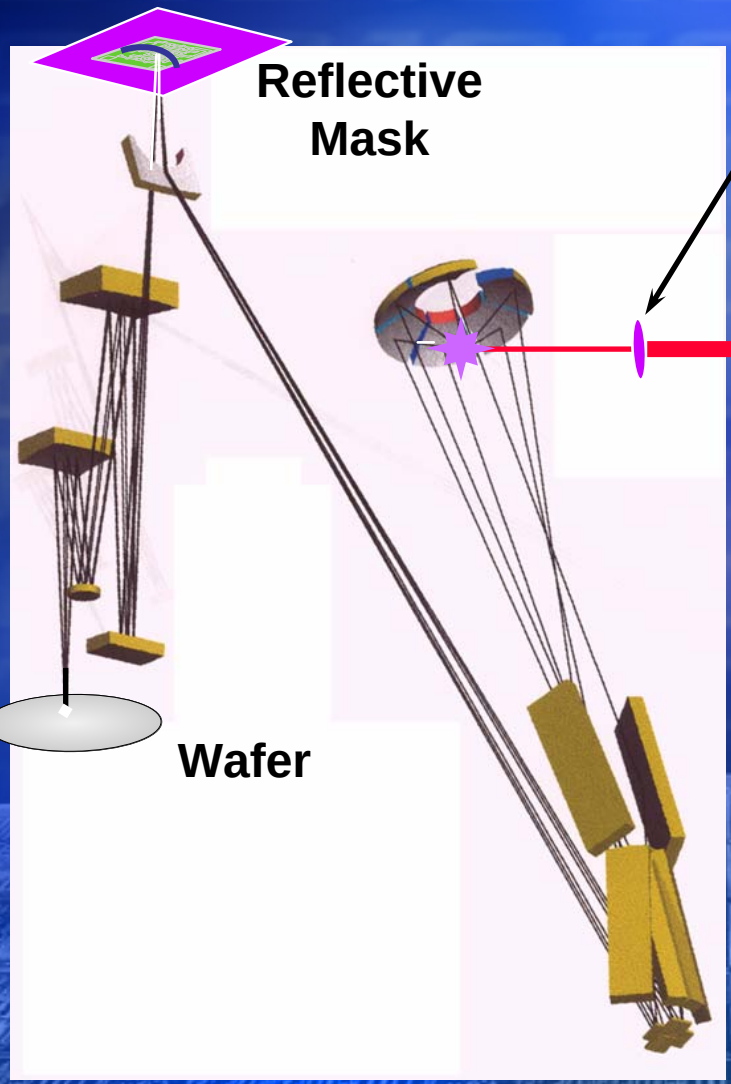
Differences

- Uses very short wavelength 13.5 nm light
- 13.5 nm radiation absorbed by all materials
- All optics are reflective
- Uses reflective masks
- No mask protective cover during exposure
- Vacuum operation
- Unique source for EUV light

EUV system



Light path in an EUV exposure tool



These differences produce new challenges

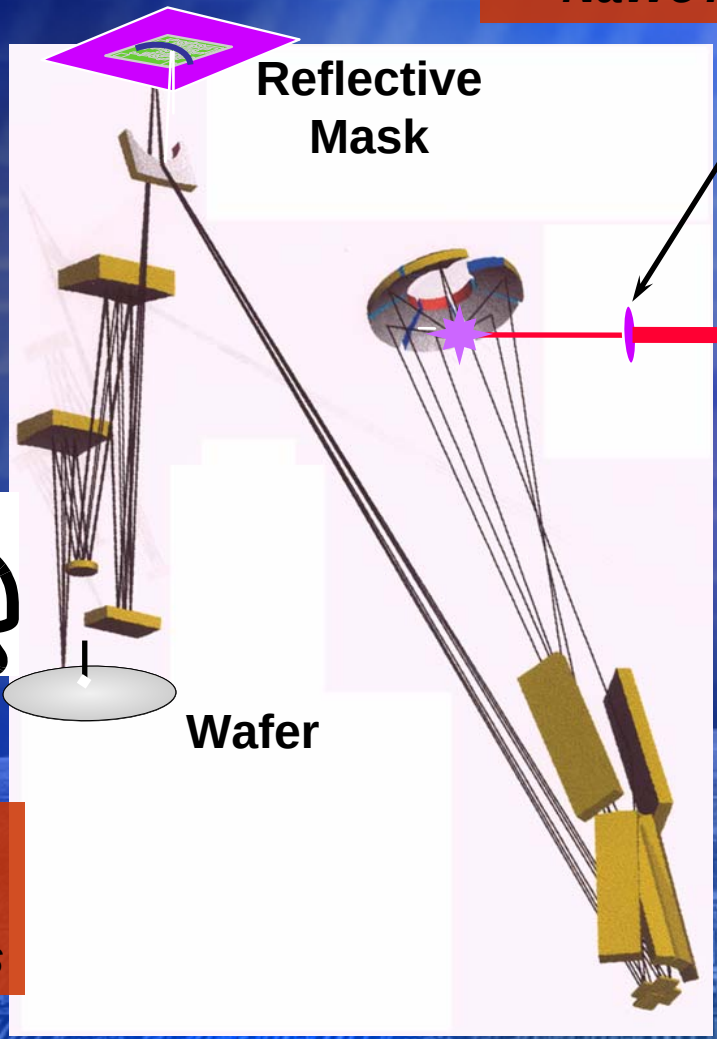
- **The development requires some different resources (suppliers, materials, researchers, …) and represents a major deviation from the conventional technology development path**

- **A major transition is required in the way the technology is developed because of the special resources and cost**

Areas highlighted in today's announcement

MET for mask defect printability

Mask Pilot Line, including NaWoTec investment

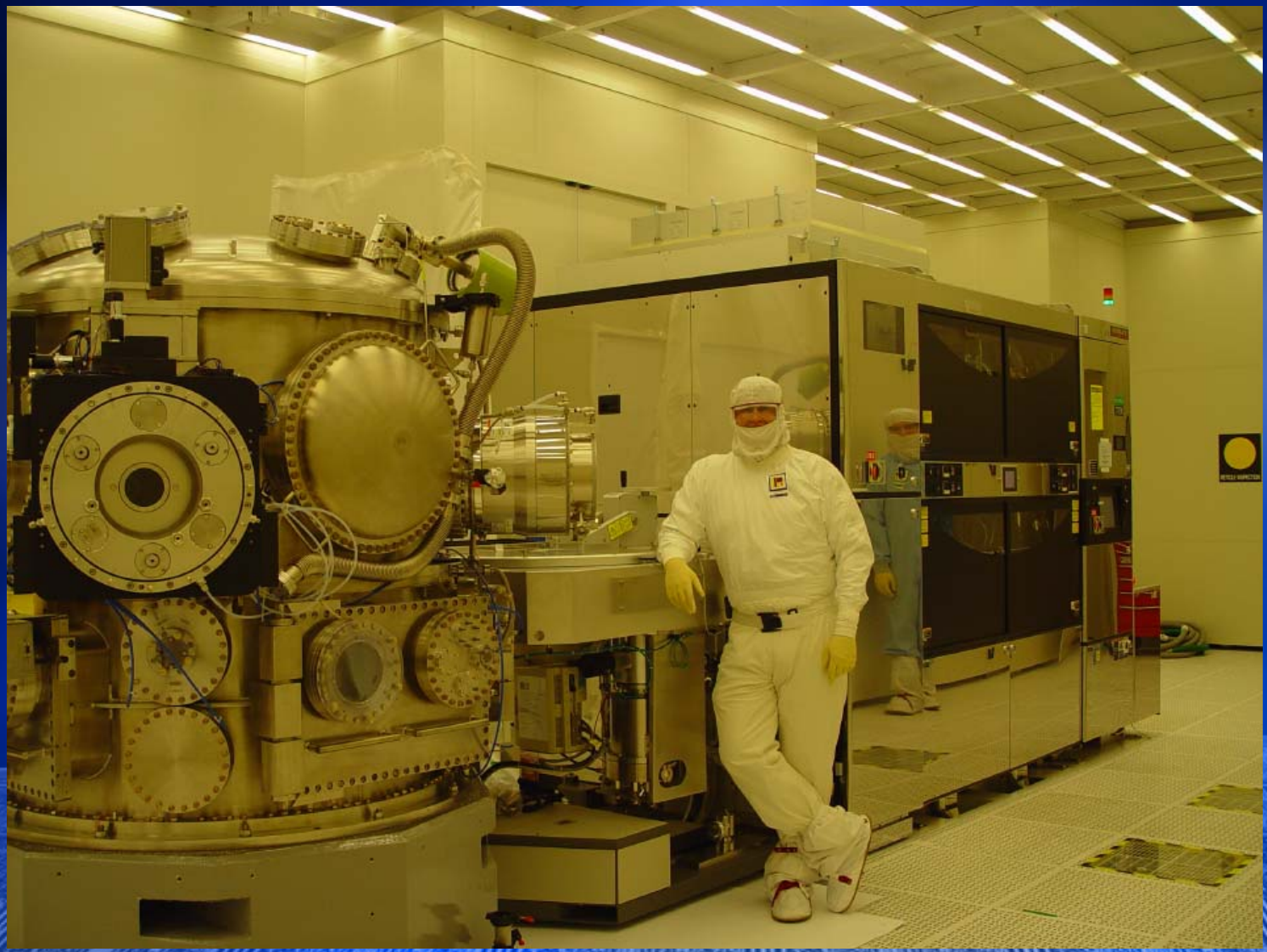


Media Lario investment

Cymer joint development program

MET for resist development and flare studies

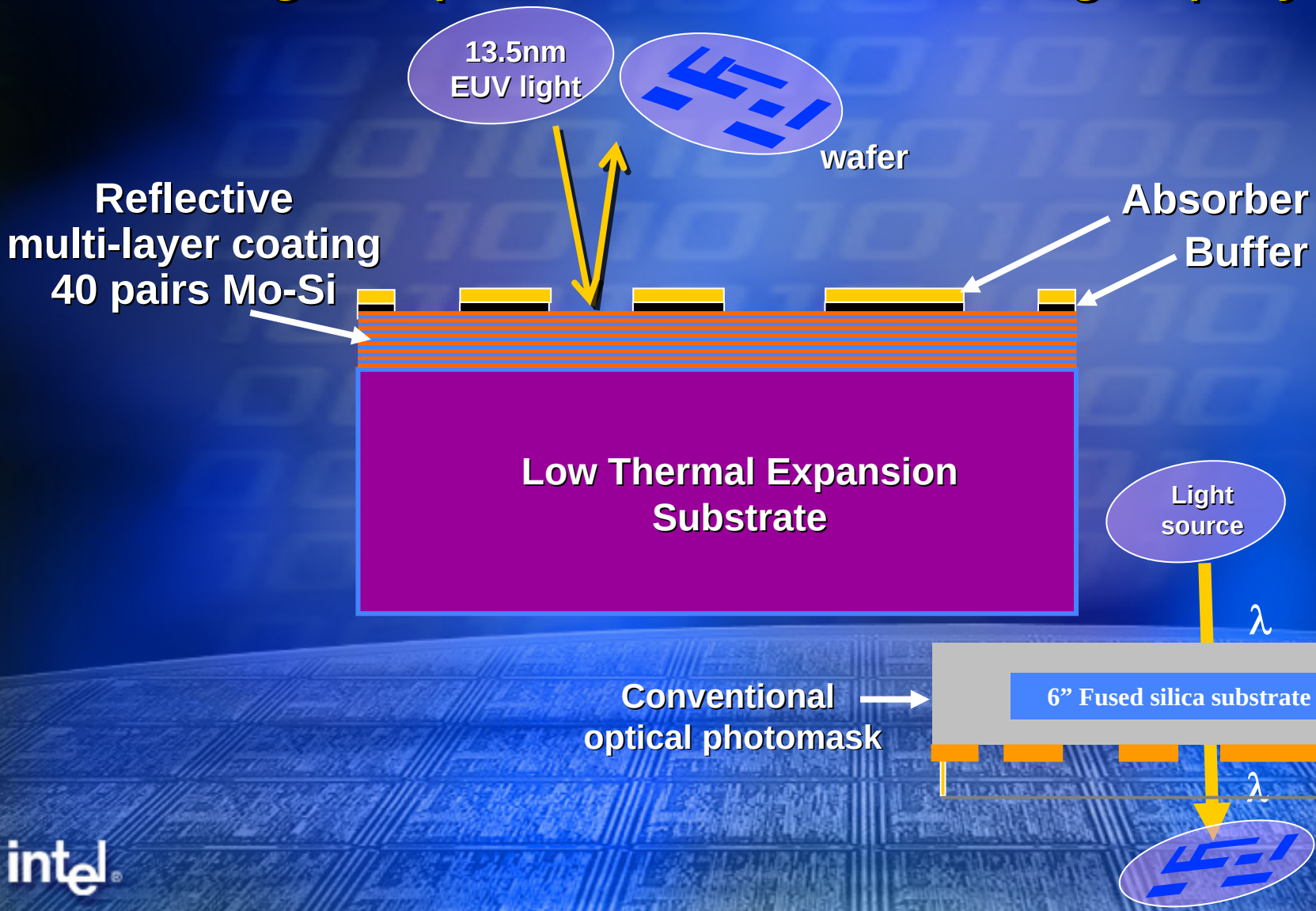
Intel's Micro Exposure Tool (MET)



Why the MET?

- **Resolution improvement**
  - **The ETS could resolve 70 nm features. The MET could resolve 30nm features.**
    This resolution improvement is necessary to develop the resist process for the feature sizes used in the 32 nm node and beyond
- **Expand resist development**
  - **EUV resist development has been limited by both exposure tool resolution and process variability stemming from manual resist processing.**
    - **Resist processing is sensitive to certain variables such as humidity, defects, thickness variation, and time to post-exposure bake, all of which can be well controlled with the linked resist track.**
      This capability allows us, then, to focus on optimizing the variables that are required for printing small features in a high volume manufacturing setting.
- **Study mask defect printability**

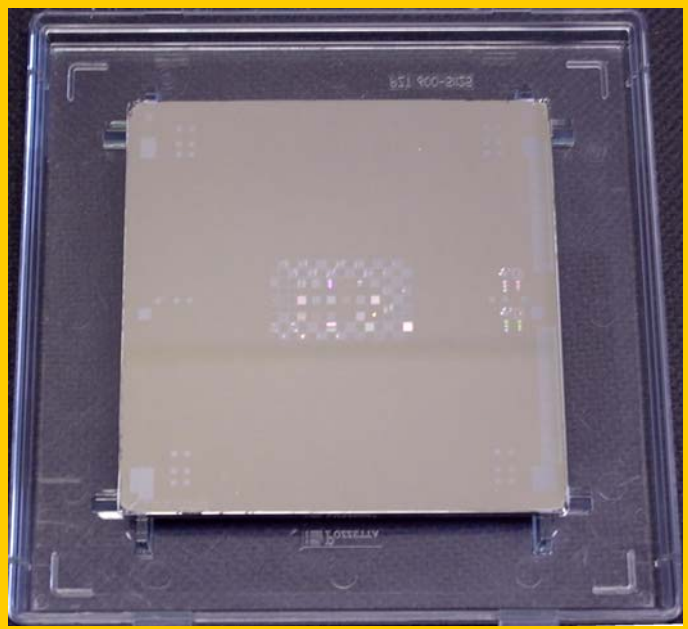
EUV Reflective Mask is an Integral part of EUV Lithography



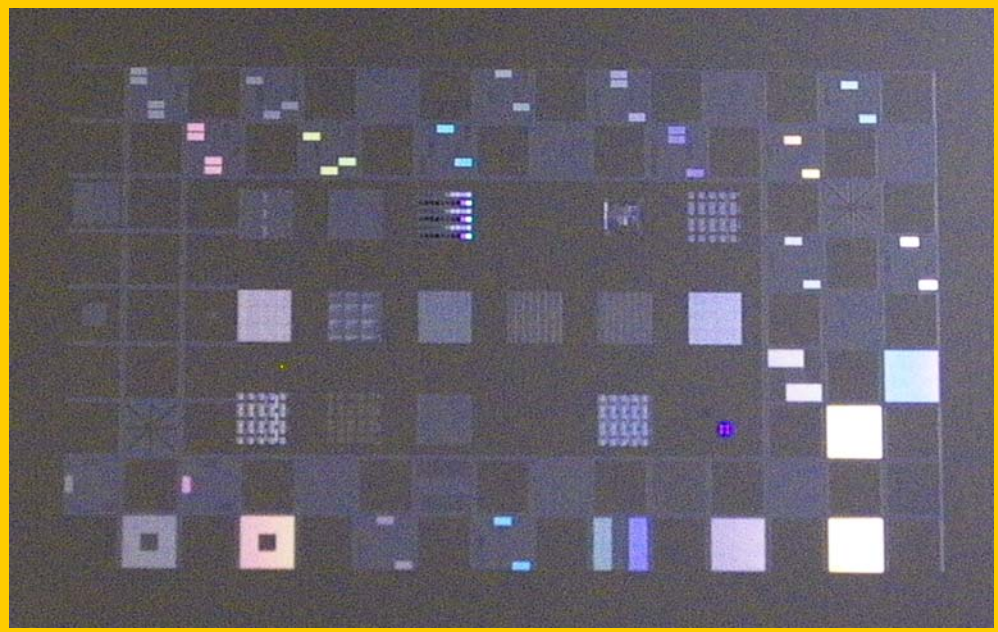
EUV Mask Pilot Line Successful Start-up

- **EUV mask pilot line integrates EUV specific modules into mask production flow**
- **This pilot line is the foundation for EUV mask development**

EUV Mask



Mask Pattern Field



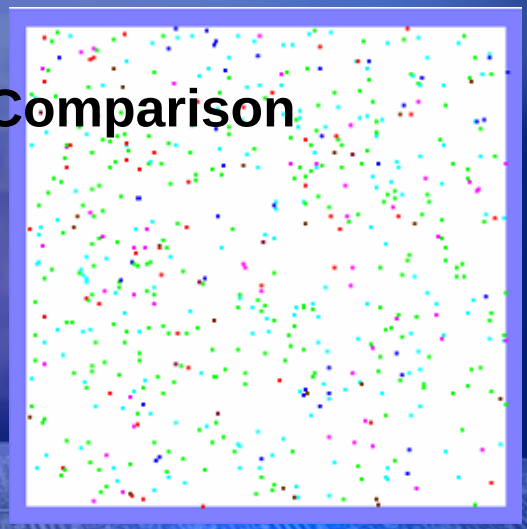
Commercial EUV Blank Defect Inspection Tool

- Intel leads the efforts on the development of this tool as industry standard
- Data are provided to suppliers for defect reduction

Commercial EUV blank inspection tool installed at Intel mask facility

Previous World Class Sensitivity (150 nm)

Defect Map Comparison

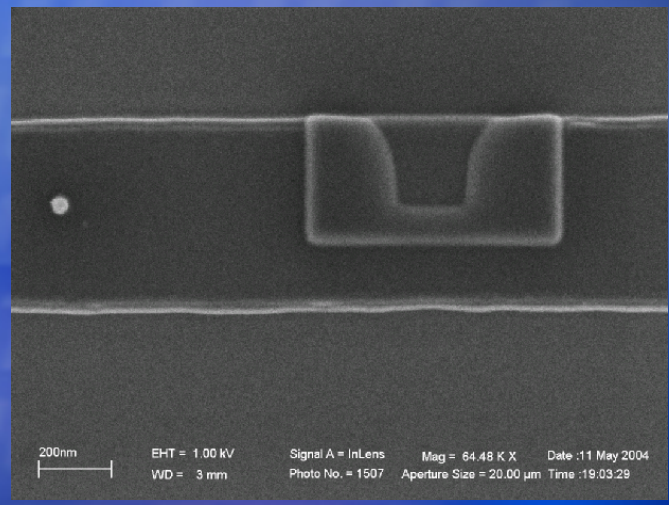


New Sensitivity (60 nm)

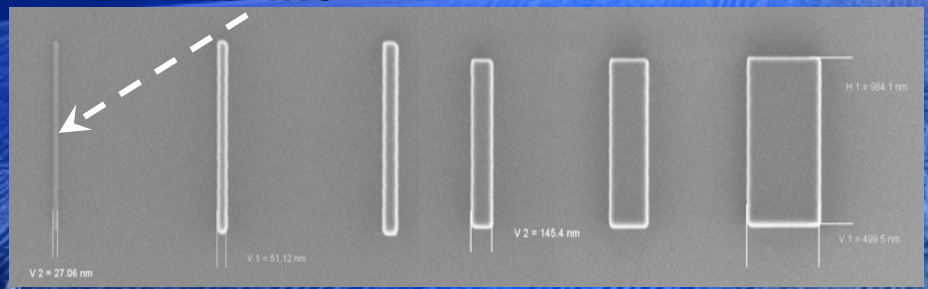
Damage-Free Repair of Patterned Masks Using Electron-beams

- **Intel co-developed this tool with NaWoTec**

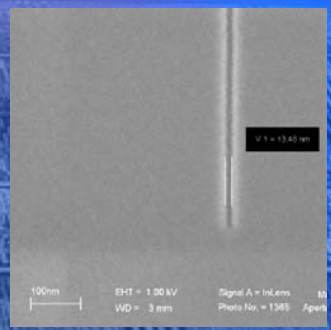
10nm (3s) position accuracy



Clear defect repair: 27 nm line



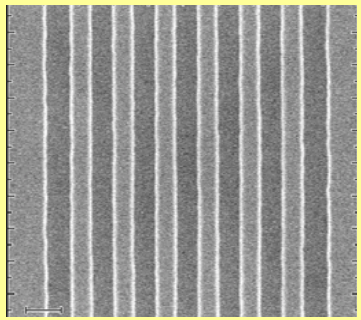
Opaque defect repair: 14nm lines etched on TaBN absorber



EUV Mask Pattern Dimensions for 32 nm Node

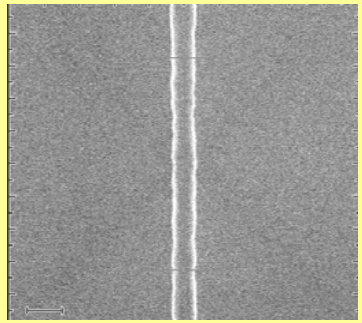
- **High resolution pilot line EUV mask for EUV MET and resist development**

1:1 L/S



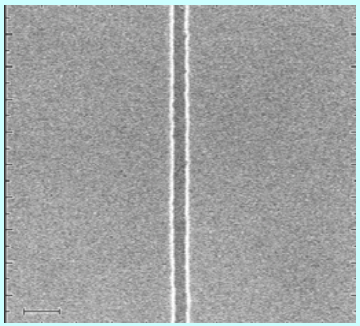
120nm l/s

Isolated lines



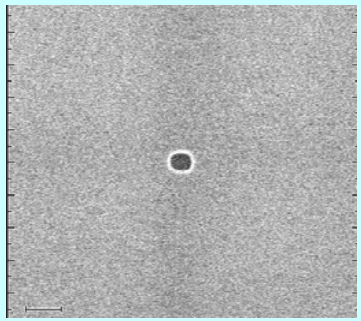
144 nm line

Isolated Space



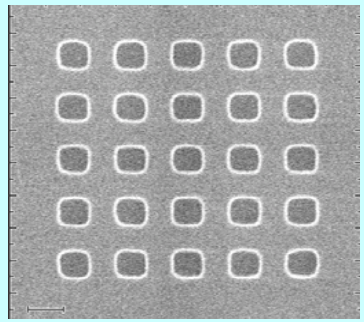
60nm space
(12nm @ wafer)

Isolated contact



120nm contact
(24nm @ wafer)

1:1 contacts

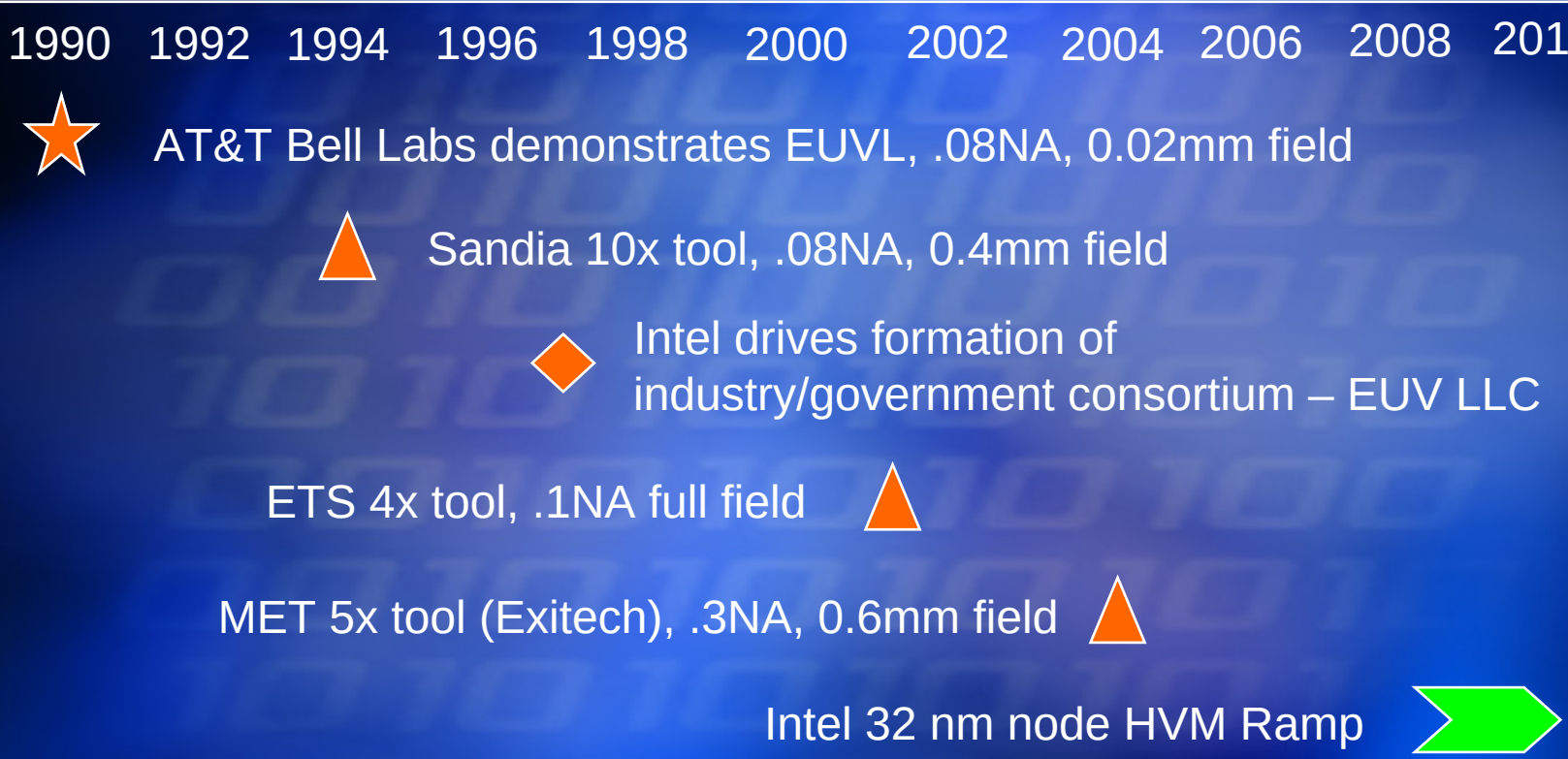


160nm contacts
(32nm @ wafer)

Why is all of this important?

- ***EXTEND*** **Intel's lithography roadmap**
- ***EXPAND*** **EUV resist development**
- ***INITIATE*** **a mask pilot production line**
- ***ENABLE*** **the EUV supplier and supplier infrastructure**

EUVL Development Timeline



Summary

- Intel reached an important milestone as it progresses toward the deployment of EUV lithography, targeted for 2009 production, with the installation of the world's first commercial EUV lithography tool, called a Micro Exposure Tool (MET).
- The MET is part of the world's first integrated EUV lithography process line and is linked with an automated track that includes resist coating and developing operations (as opposed to stand-alone tools), indicating that this technology is moving out of the research lab toward a pilot line environment.
- Intel plans to develop its EUV masks in-house, and to that end has successfully established an EUV mask pilot line, including the world's first commercial EUV mask making tools, an e-beam mask repair tool and a mask blank defect inspection tool.
- The results announced today show that Intel is positioned to be the first company to deploy EUV lithography, further extending Moore's Law into the next decade.

intel

For further information on Intel's silicon technology and Moore’s Law, please visit the Silicon Showcase at www.intel.com/research/silicon