6.004 Computation Structures
Spring 2009

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

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Quiz #2: March 13, 2009

Name	*Athena login name*	*Score*
Solutions		Avg: 19.0

Problem 1 (4 points): **Quickies and Trickies**

(A) A latch is constructed from a 2-input lenient MUX having a propagation delay of 200ps and a contamination delay of 20ps, using the design shown in lecture. Give the minimum appropriate setup time specification for this latch.

Setup time (ps): 400

(B) Give the best achievable asymptotic throughput for a pipelined multiplier capable of multiplying two N-bit operands. Enter a number, a formula, or "CAN'T TELL".

Asymptotic throughput: $\Theta($ 1 $)$

(C) A complex combinational circuit is constructed entirely from 2-input NAND gates having a propagation delay of 1 ns. If this circuit is pipelined for maximal throughput by adding registers whose setup time and propagation delay are each 1 ns, what is the throughput of the resulting pipeline? Enter a number, a formula, or "CAN'T TELL".

Throughput (ns^{-1}): 1/3

(D) A "Thingee" is a clocked device built out of 3 interconnected components, each of which is known to be a 4-state FSM. What bound, if any, can you put on the number of states of a Thingee?

Max # of states, or "Can't Tell": 64

Problem 2 (6 points): **Reliability measures**

Your thesis supervisor has offered you a number of candidate topics, each involving the construction of a gadget from reliable electronic components. To select a project, you decide to evaluate, for each choice, whether it can be made to meet its specification with perfect reliability. Each device takes two digital inputs A and B, each of which start at logical 0 and have a single positive transition at t_A and t_B, respectively. The propagation delay t_{pd} is to be 1 nanosecond.

(A) The output Q is guaranteed to be a valid 1 or 0 t_{pd} after the second input transition, but there is no constraint on which value is output.

Can be made reliable? Circle one: YES … NO … CAN'T TELL

(B) The output Q is guaranteed to be a valid 1 or 0 t_{pd} after the second input transition, must be 1 if t_A is 10ns or more ***earlier*** than t_B, must be 0 if t_A is 10ns or more ***later*** than t_B, or otherwise can be either valid logic level.

Can be made reliable? Circle one: YES … NO … CAN'T TELL

(C) At t_{pd} after the second input transition, the output Q must be a valid 1 if t_A is 10ns or more ***earlier*** than t_B, must be a valid 0 if t_A is 10ns or more ***later*** than t_B, and is otherwise unspecified (may be invalid) if t_A and t_B are within 10 ns of each other.

Can be made reliable? Circle one: YES … NO … CAN'T TELL

(D) Prior to t_A and t_B the output Q must be a valid 0, but it must become a valid 1 within t_{pd} of the first input transition.

Can be made reliable? Circle one: YES … NO … CAN'T TELL

(E) The output Q is guaranteed to be a valid 1 or 0 t_{pd} after the second input transition, must be 1 if the transitions are within 10ns of each other, and must be 0 if the transitions are separated by more than 20ns.

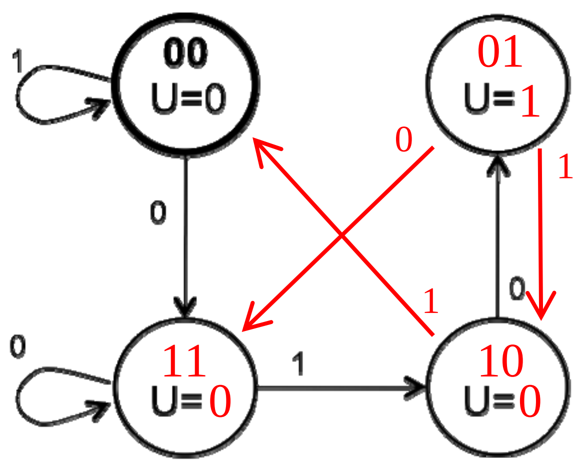
Can be made reliable? Circle one: YES … NO … CAN'T TELL

(F) Two outputs, Q and R, where R is guaranteed to become a valid 1 sometime after the first input transition. When R=1, the Q output must be a valid 1 if t_A is 10ns or more ***earlier*** than t_B, must be a valid 0 if t_A is 10ns or more ***later*** than t_B, or otherwise may be either valid logic level.

Can be made reliable? Circle one: YES … NO … CAN'T TELL

Problem 3. (9 Points) **Picking Locks, 6.004 style**

Perfectly Perplexing Padlocks makes an entry-level electronic lock, the P3b, built from an FSM with two bits of state. The P3b has two buttons ("0" and "1") that when pressed cause the FSM controlling the lock to advance to a new state. In addition to advancing the FSM, each button press is encoded on the B signal (B=0 for button "0", B=1 for button "1"). The padlock unlocks when the FSM sets the UNLOCK output signal to 1, which it does **whenever—and only whenever—the last 3 button presses correspond to the 3-digit combination**. The combination is unique, and will open the lock independently of the starting state.
Unfortunately the design notes for the P3b are incomplete.



S_1	S_0	B	S'_1	S'_0	U
0	0	0	1	1	0
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	1	0	0

(A) (1 Point) What is the 3-bit combination for the lock?

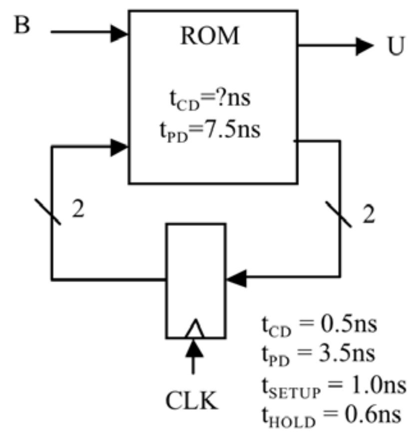
lock combination:_____010_____

(B) (4 Points) Using the specification and clues from the partially completed diagrams above fill in the information that is missing from the state transition diagram and its accompanying truth table. When done:

- each state in the transition diagram should be assigned a 2-bit state name $\mathbf{S_1S_0}$ (note that in this design the state name is *not* derived from the combination that opens the lock),
- the arcs leaving each state should be mutually exclusive and collectively exhaustive,
- the value for **U** should be specified for each state, and
- the truth table should be completed.

(complete above transition diagram and table)

The circuit diagram for the P3b is shown below. You may assume that the B input has been appropriately synchronized with CLK.



(C) (1 Point) How many bits are stored in the ROM?

Total size of ROM, in bits: 24

(D) (1 Point) What is the smallest value for the ROM's contamination delay that ensures the necessary timing specifications are met?

smallest valid value for $t_{CD,ROM}$ (ns): 0.1

(E) (1 Point) What is the smallest value for the period of CLK that will meet the timing specifications?

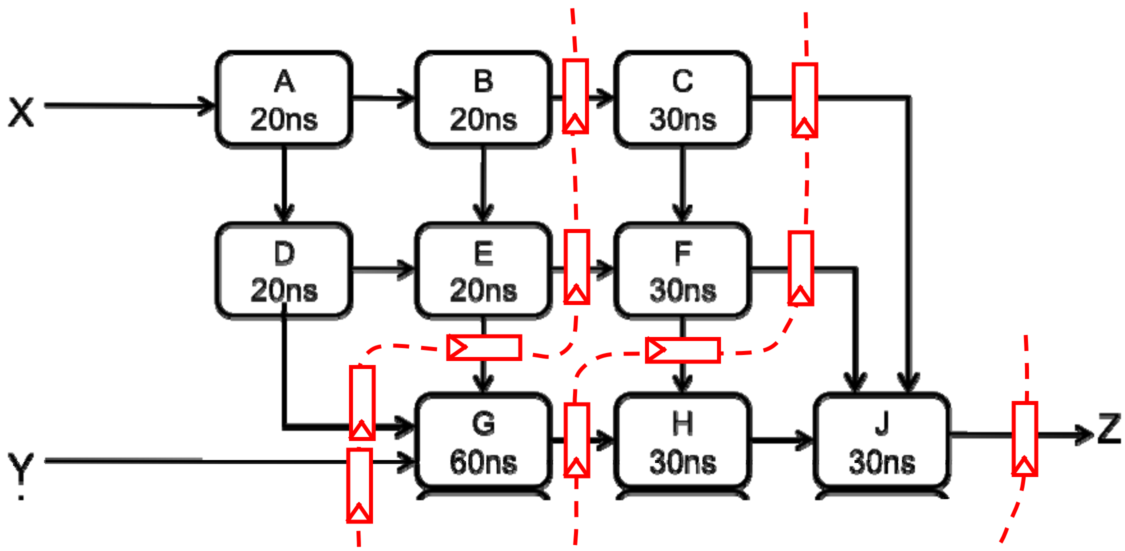
smallest value for t_{CLK} (ns): 12

(F) (1 Point) What is the smallest setup time for the B input with respect to the active edge of CLK that ensures the necessary timing specifications are met?

smallest setup time for B input (ns): 8.5

Problem 4 (6 Points) **The Mysterious XYZ Machine**

An unidentified government agency has a design for a combinational device depicted below:



Although you don't know the function of each of the component modules, they are each combinational and marked with their respective propagation delays. You have been hired to analyze and improve the performance of this device.

NOTE: Scratch copies of the above diagram appear on the back of the previous page.

(A) (1 Point) What are the best throughput and latency that can be achieved with the combinational device?

Latency: 180 **ns; Throughput:** 1/180 **ns**$^{-1}$

(B) (4 Points) Show how to pipeline the above circuit for maximum throughput, by marking locations in the diagram where registers are to be inserted. Use a minimum number of registers, but be sure to include one on the output.

(mark register locations in diagram above)

(C) (1 Point) What are the latency and throughput of your pipelined circuit?

Latency: 180 **ns; Throughput:** 1/60 **ns**$^{-1}$

END OF QUIZ!